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System Description
Of the
RF Control System
(RFCS)
For the
Spallation Neutron Source

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1.01	Minor mods to REF description. DWT 10/20/00
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Open Items

Ref	Section	Item	Closed
1	2.2	Define RFCS-HEBT Interfaces.	
2	2.4	Describe SRF cavity resonance control function	12/14/00 by AHR
3	3.	Define RFCS-Event Link Module Interface	
4	3.	Define RFCS-MPS Module Interface. Define how many MPS modules per crate.	06/18/01 by DWT
5	3.1.3	Clarify timing between PREPULSE and RF_GATE*	06/18/01 by DWT
6	4.1	Select/Define feedforward control strategy	
7	4.2.2	Provide example of SRF resonance control function.	06/18/01 by AHR
8	4.4.1	Define all operating modes. Separate static modes from dynamic modes.	
9	4.10	Define FRCM-EPICS interfaces.	
10	5.4.1	Define HPM ADC latency.	
1	5.5	Define HPM FOARC input/output delay	
12	5.5	Define HPM FOARC input connector.	12/14/00 by DWT
13	5.6.1	Define RF_PERMIT to FAULT_L/R* delay.	
14	5.6.1	Define RF_PERMIT input connector.	12/14/00 by DWT
15	5.6.2	Define FAULT_L/R* to RF_FAULT* delay.	
16	5.6.2	Define RF_FAULT* output connector.	12/14/00 by DWT
17	5.9	Define HPM – EPICS interfaces.	06/18/01 by DWT
18	6.5	Define CDM – EPICS interfaces.	06/18/01 by AHR
19	7.2	Define REF – EPICS interfaces REF Temperature Controller REF Pressure Controller REF RF status reporting Define a home for the REF temperature controllers.	
20	7.2	Define REF BIT functions	
21	Appendix One	Define interconnect cables for each subsystem.	11/21/00 by DWT

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Introduction

This document describes the Low Level RF Control System (RFCS¹) for the National Spallation Neutron Source (SNS) to be built at Oak Ridge National Laboratory (ORNL) by the RF Controls Group (SNS-2) of Los Alamos National Laboratory (LANL). This document begins with a general description of the RFCS and its context within the overall SNS LINAC and then describes each subsystem in detail. Comments or corrections should be referred to Amy Regan or Dave Thomson at LANL.

¹ A table of acronyms appears in an appendix.

1 System Overview

1.1 Radio Frequency Control System

The primary function of the Radio Frequency Control System (RFCS) is to provide the correct (frequency, amplitude, and phase) radio frequency carrier to the RF transmitter system for the SNS LINAC. Secondary functions are to protect the High Power RF system from RF faults and to manage the resonant frequency of the various accelerator cavities. Table 1-1 describes the fundamental accelerator design parameters that directly drive the operational requirements for the RFCS.

Table 1-1. Fundamental Accelerator Parameters

Parameter	Value
Pulse Rep Rate	60.0 Hz (and, possibly, 10.00 Hz interleaved) What about 120 HZ Modes?
MacroPulse Width	0.945 ms (645 ns ON/300 ns OFF), 1.1886 MHz
LINAC Length	Approximately 335 m
RFQ Resonance Control Requirement	F ₀ : 402.5 MHz ± 15 kHz; Q _L = 3,300 BW = 122 kHz
DTL Resonance Control Requirement	F ₀ : 402.5 MHz ± 2 kHz Q _L : 17,818 (smallest bandwidth case) BW = 23 kHz
CCL Resonance Control Requirement	F ₀ : 805 MHz ± 10 kHz Q _L : 8,108 (smallest bandwidth case) BW = 99 kHz
SRF β=0.61 Resonance Control Requirement	F ₀ : 805 MHz ± 500 Hz Q _L : 733,000 BW = 1 kHz
SRF β=0.81 Resonance Control Requirement	F ₀ : 805 MHz ± 500 Hz Q _L : 699,000 BW = 1 kHz
Field Control Requirement, all cavities	<u>Amplitude Tolerance</u> : ± 0.5% Max in steady state, ± 0.75% during beam turn-on transient. <u>Phase Tolerance</u> : ± 0.5° Max in steady state, ± 0.75° during beam turn-on transient.

Table Notes:

1. DTL and CCL data updated from James Billen (October 16 and 18, 2000).
2. Bandwidth in the table is the double-sided bandwidth (F₀/Q_L). In our models (and TESLA's TTF) we use the single-sided BW (F₀/2Q_L).

1.2 System Errors

The major system errors are shown below in Figure 1-1. Because the primary purpose of the RFCS is to minimize deviations of the cavity field amplitude and phase from their respective setpoints, the system errors are referenced to the feedback loop comparison point.

Any shift in differential transmission phase among the various RF reference transports in the SNS system will translate directly to errors in cavity-to-cavity phase. The error contribution shown for the sense transport includes the amplitude and phase errors from both the transport line and the detection electronics that it feeds. The performance

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objectives and tolerance budget for these systems have been allocated as shown in Table 1-2, where E_r , E_s , and E_c are defined in Figure 1-1.

Figure 1-1. Error Signals

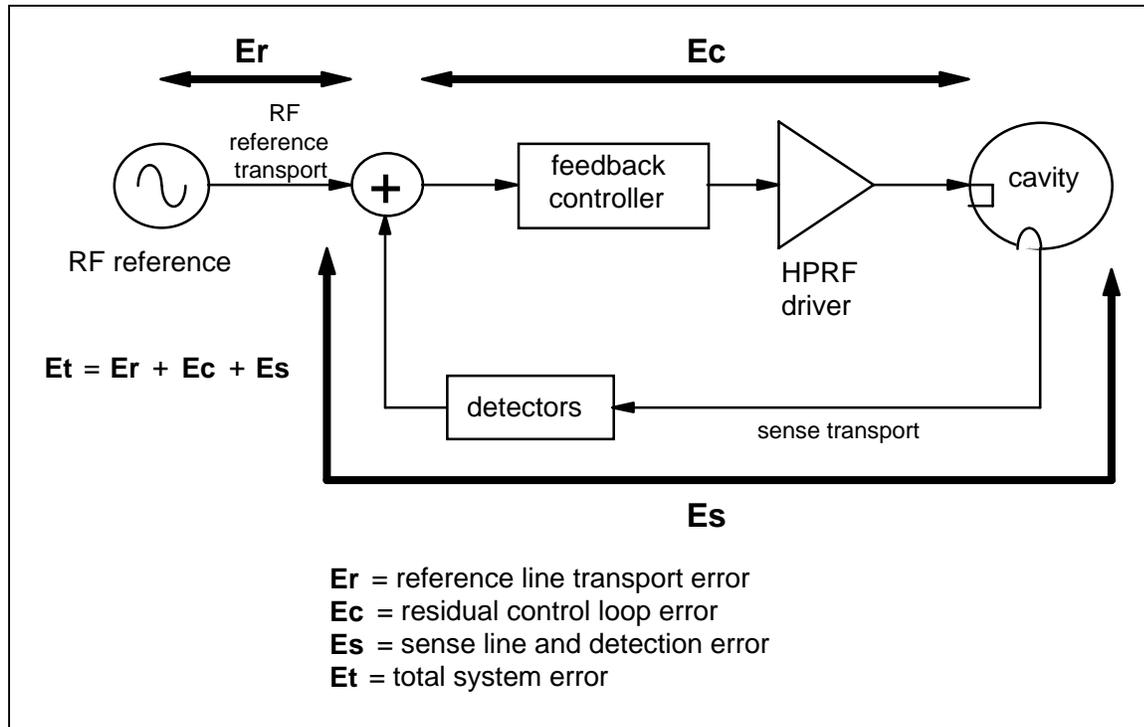


Table 1-2. Amplitude and Phase Tolerance Budget

	AMPLITUDE (%)	PHASE (°)
E_r	N/A	± 0.15
E_s	± 0.2	± 0.15
E_c	± 0.3	± 0.2
Total	± 0.5	± 0.5

1.3 SNS LINAC Architecture

The SNS LINAC consists of six major segments: an injector/RF quadrupole (RFQ), a drift tube LINAC (DTL), a coupled-cavity LINAC (CCL), a superconducting low beta segment, a superconducting high beta segment, and a high-energy beam transport (HEBT) segment. All LINAC segments operate at room temperature (NC, normal conducting) except for the two superconducting (SRF) sections. Each subsystem has its own high power klystron RF amplifiers and each klystron has its own RFCS subsystem (VXibus Crate). See Table 2- 1 for a summary of the RFCS requirements.

1.4 RFCS Subsystems

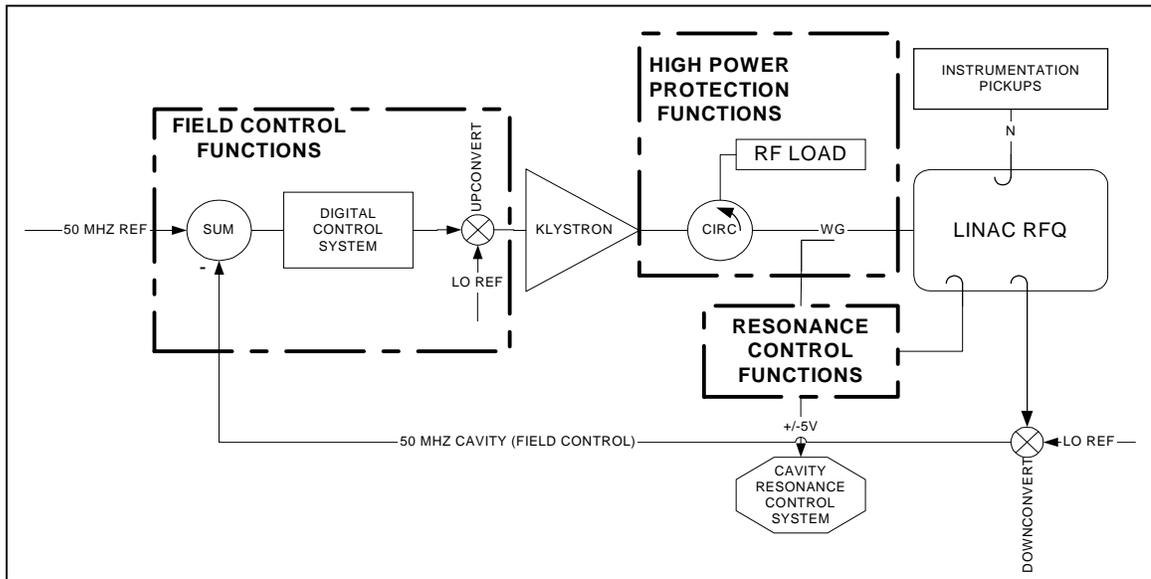
The four primary functions of the RFCS are control of the cavity fields (Field Control), detection and control of the cavity resonance (Resonance Control), protection of the

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klystrons and cavities from high power faults (High Power Protection) and the radio frequency reference distribution subsystem. See Figure 1-2.

The RF Control system will maintain the SNS LINAC (and RFQ and HEBT) cavity field amplitudes (voltage) to within ± 0.5 percent and ± 0.5 degrees in steady state in the presence of beam over the approximately 335 m length of the accelerator.

Figure 1-2. System Functional Block Diagram



The selected architecture for the RF Control System is VXIbus. Each of these global RF control functions, with the exception of the Reference Generation and Distribution, will be located on a VXIbus module. In broad terms, the Field, Resonance, and Amplifier Control functions are performed by a Field / Resonance Control Module (FRCM) in conjunction with a Clock Distribution Module (CDM); and the High Power Protect function is performed by a HPRF Protect Module (HPM). Figures 2-1 through 2-4 show how these modules are connected in the various stages of the LINAC, while Table 2-1 summarizes the total module requirements. The VXIbus interfaces are described in more detail in Section 3 of this document.

1.4.1 Field / Resonance Control Module (FRCM)

The FRCM performs both feedback and feedforward control on an error signal generated by the comparison of a cavity field sample and the operator-defined set point. It utilizes this control signal to provide a corrected drive signal to the klystron. In addition, the FRCM continuously monitors the actual cavity resonance frequency and, depending on the magnitude of the error between the actual resonance frequency and the desired operating frequency, takes actions to move the cavity resonance to the operating frequency, either by slewing the drive frequency, issuing a correction signal to the Resonant Cavity Control System (RCCS), or both. The FRCM is described in more detail in Section 4 of this document.

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1.4.2 High Power Protection Module (HPM)

The High Power Protection Module (HPM) continuously monitors the high power RF distribution system using RF power detectors and fiber optic arc detectors. It also provides the interface between the RFCS and the global SNS Machine Protection System. The HPM is further described in Section 5 of this document.

1.4.3 Clock Distribution Module (CDM)

The Clock Distribution Module (CDM) generates the master timing signals for the other LANL modules in the VXIbus crate. It also receives timing information from the Brookhaven National Laboratory's (BNL) Event Link and Timing Modules and reformats it for the TTLBUS on the crate backplane for use by the various modules. The CDM is described in more detail in Section 6 of this document.

1.4.4 Frequency Reference System (REF)

The key to operating the accelerator RF control system is a stable frequency reference distributed to the various control racks. The reference system is designed to maintain a total phase error in the reference frequencies of $\pm 0.1^\circ$ over the entire length of the accelerator. To minimize the error contribution of the frequency reference system, the reference signals are distributed in insulated, temperature-controlled coaxial lines. The frequency reference system is described in more detail in Section 7 of this document.

1.4.5 RFQ Multiplexers

The RFQ section of the LINAC (see Figure 2-1) has eight drive ports with a forward and reflected directional coupler at each port. Additionally, there are 16 field taps arrayed along the cavity. The RFQ RFCS includes two 16:1 double-slot wide VXIbus solid state multiplexers, controlled *via* EPICS to select either forward/reverse power pairs or two simultaneous pairs of cavity field probes. The two selected outputs are then fed to the HPM for power monitoring *via* an EPICS screen. The multiplexers are further described in Section 8 of this document.

1.4.6 IOC – VXIbus Crate Controller

The MVME2100 Power PC has been selected by the Controls group as the standard IOC (Input/Output Controller) for the RFCS. Its use and limitations are described in Sections 3.1 and 9 of this document.

1.4.7 Brookhaven National Laboratory Timing Module

System timing is managed by a Brookhaven National Laboratory-designed V124s timing module that is co-located in the RFCS crate with the rest of the equipment. Its functions are more fully described in Section 3 of this document.

1.4.8 VXIbus Crate

The VXIbus crate provides the “home” for the RFCS in the SNS system. It was selected for its superior power supply and cooling capabilities, which were dictated by the requirement of putting two FRCM cards in a single crate. These are high power-dissipation cards, and there are few crates that are rated to dissipate the heat they generate. The crate is further described in Section 10 of this document.

2 RF Control System Interconnection Block Diagrams

The following block diagrams emphasize the cabling between the RFCS and the high power RF systems. For the most part, these RF cables are 3/8" Heliax between the tunnel and the top of the RFCS rack (N-Male to N-Male), and then more flexible cable (Times LMR-195 N-Female to PKZ) between the rack-top patch panel and the front panel of the RFCS modules. The standardized maximum RF power level at the RFCS rack-top is +20 dBm. The standardized maximum RF power level at the front panel connectors of the RFCS is +10 dBm, adjusted *via* fixed N-connector pads at the patch panel. Cable interconnection tables may be found in Appendix Three. A summary of the various input and output requirements may be found in Table 2 - 1.

2.1 RFQ RFCS Cabling Block Diagram

Figure 2-1. RFQ RFCS Cabling Block Diagram

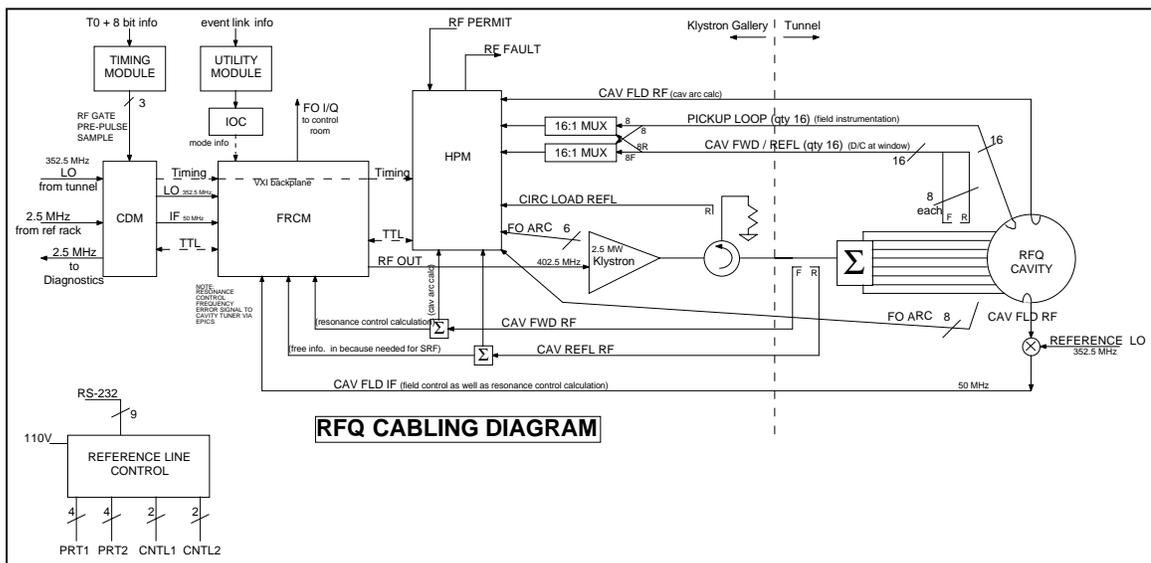


Figure 2-1 shows the cabling block diagram for the RFQ (RF Quadrupole) portion of the LINAC. The BNL-designed Utility Module monitors the Event Link (a system that broadcasts to the accelerator control system critical operating parameters on a pulse-by-pulse basis) and asserts an interrupt to the IOC on receipt of a valid message. The IOC services the interrupt and writes it to a mailbox register in the FRCM, telling the FRCM the mode of the upcoming pulse.

The CDM receives a reference 2.500 MHz signal from the frequency reference system rack and the 352.5 MHz LO (local oscillator) reference signal from the REF line in the tunnel. These signals are then converted to clock, IF, and LO signals for use by the FRCM and the HPM. The CDM also receives timing signals from the Brookhaven timing module and distributes them to the HPM and FRCM. The CDM is further described in Section 6 of this document.

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The FRCM receives a precision 50 MHz IF feed from a cavity field probe signal (CAV_FLD_IF²) which has been down-converted in the tunnel to provide a signal for the cavity field and resonant frequency calculations, along with signals representing the RF power into the cavity 8-way splitter (CAV_FWD_RF) and the RF power reflected from the cavity splitter (CAV_REFL_RF). These two RF signals are split at the RFCS rack-top to also feed the HPM.

An important function of the FRCM is to manage the cavity center frequency by detecting the frequency error (deviation from the design point) and transmitting the error signal *via* EPICS to the Resonant Cavity Control System. This function is further described in Section 4.2 of this document.

Each FRCM also has a digital fiber optic data link to provide simultaneous serial I and Q data to the control room for diagnostics. These signals are received and converted to analog voltages in the control room for display on an oscilloscope to assist in commissioning and trouble-shooting.

The primary function of the HPM is to interface the various RF signals from the high power waveguide distribution system with the RFCS and EPICS. These RF inputs are monitored and, if they indicate a fault, the HPM kills the RF carrier for the duration of the macropulse and notifies the MPS of the fault condition. A secondary function of the HPM is to interface the waveguide fiber optic arc detectors (FOARC, managed by the High Power RF Group) with the MPS and blank off the RF carrier for the duration of the macropulse when a waveguide arc is detected.

The HPM has two opto-isolated interfaces with the “outside world” for quick-response functions. The first is with an unknown control system (TBD) that provides the HPM with an RF_PERMIT input. The second interface (RF_FAULT) is with the machine protection system (MPS). The HPM provides a quick (microsecond scale) alert to the MPS of an RF fault, bypassing the EPICS system. The HPM is further described in Section 5 of this document.

The HPM (for the RFQ only) also digitizes the inputs from 32 RF probes in the RFQ cavity and waveguide distribution system. The 16 cavity field probes are split between two 16:1 solid state, VXIbus-controlled RF multiplexers, the outputs of which are supplied to the HPM for digitizing and monitoring. The eight forward and eight reflected power probes are also supplied to the multiplexers, the eight forward to multiplexer one and the eight reflected to multiplexer two. This permits observing the forward and reflected powers simultaneously at each of the cavity port directional couplers.

There are eight Reference Line Temperature controllers in the entire SNS system. These monitor and control the temperature of the reference distribution line by switching flexible strip heaters on and off. These controllers communicate with the RFCS IOCs *via* an RS-232 communication link. The reference system is further described in Section 7 of this document.

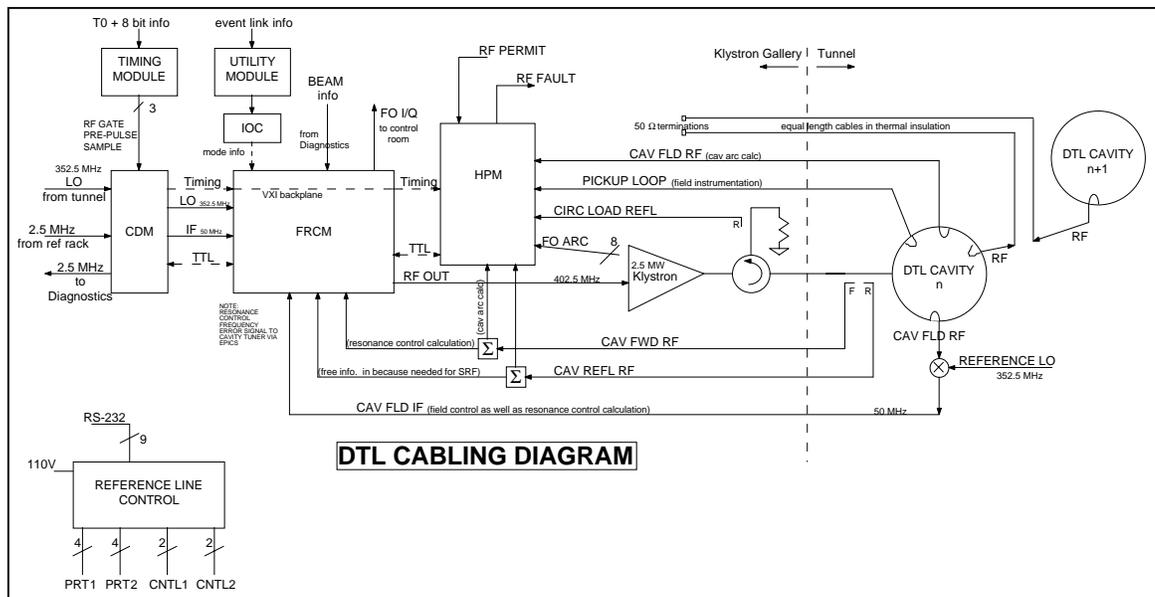
² Signal names are in THIS_FONT

2.2 DTL and HEBT RFCS Cabling Block Diagram

Figure 2-2 shows the typical interface diagram for the DTL (Drift Tube LINAC) and HEBT (High Energy Beam Transport) portions of the RFCS. The modules (Timing Module, CDM, FRCM, HPM) are the same as before (although possibly with different firmware, specific to the cavity characteristics). The I/O to the CDM and FRCM are the same as before. The HPM I/O is slightly different in that there are only 5 RF and 8 FOARC channels used. In addition, a pair of equal-length bundled and insulated cables are brought up to the gallery from taps on adjacent cavities. These will be used to monitor (and tune) the phase advance of the RF carrier from cavity to cavity during cavity commissioning.

The HEBT (High Energy Beam Transport) interfaces are **TBD**. The assumption is that they are sufficiently similar to the DTL interfaces that no hardware changes (other than compensating for the change in operating frequency from 402.5 to 805 MHz) will be required.

Figure 2-2. DTL and HEBT RFCS Cabling Block Diagram

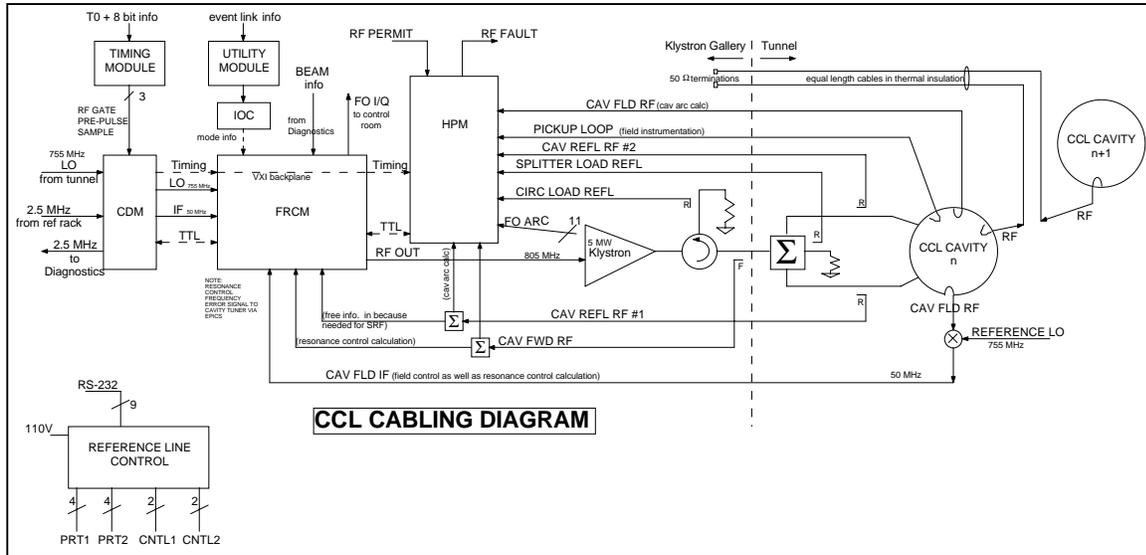


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2.3 CCL RFCS Cabling Block Diagram

The RFCS interfaces to the CCL (Coupled Cavity LINAC) are shown in Figure 2-3. It differs primarily from the previous configurations in that the HPM monitors the reflected power from the two cavity feed points separately to detect a cavity arc. The cavity arc detection algorithm is described in Section 5.2.1.

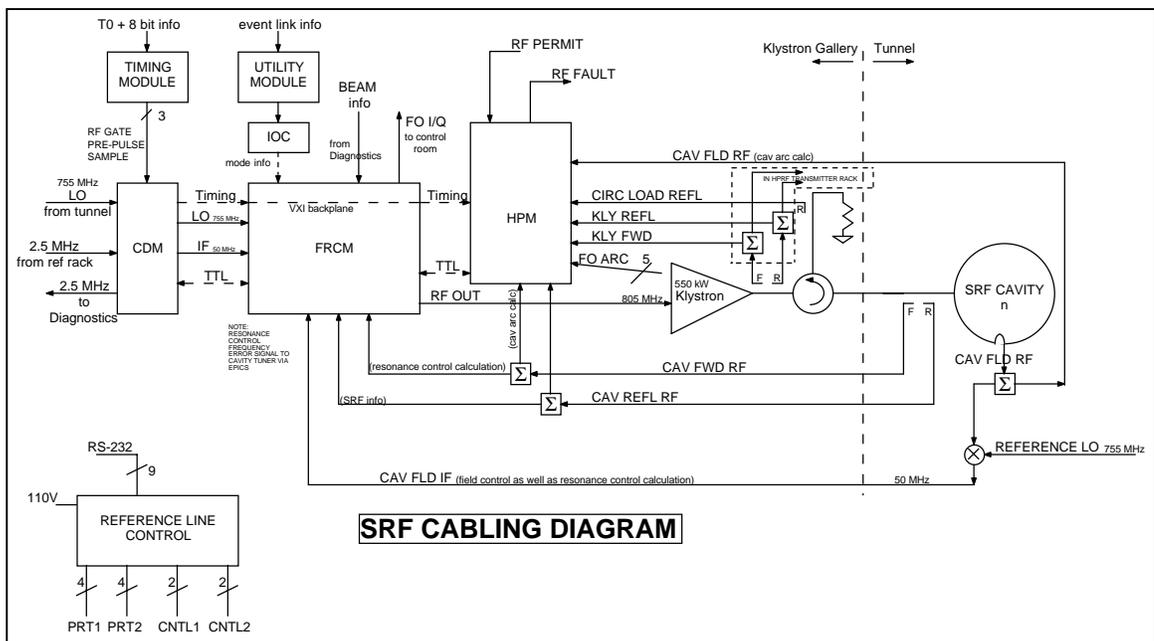
Figure 2-3. CCL RFCS Cabling Block Diagram



2.4 RF RFCS Cabling Block Diagram

The interfaces between the RFCS and the superconducting RF (SRF) cavities are shown in Figure 2-4. While the general topology is familiar, we split the single cavity field probe two ways to serve the FRCM downconverter and the HPM cavity field reference channel to avoid additional cavity probe penetrations. The resonance control function is accomplished by a mechanical compression of the cavity driven by a stepper (or servo) motor. The FRCM provides a frequency error signal to EPICS, which value is then used by the motor controller to either compress or expand the cavity to bring it into resonance. The klystron forward and reflected power signals are split at the High Power RF rack and sent to the HPM *via* cables in the klystron gallery.

Figure 2-4. SRF Medium and High Beta RFCS Cabling Block Diagram



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Table 2-1. SNS RFCS Quantities and Certain External Signals

Accelerator Stage	RF Frequency (MHz)	NC RFCS Systems	SRF RFCS Systems	Cavity Field RF + IF	Cavity Drive FWD + RFL Power	Klystron FWD + RFL Power	Circulator + Splitter Load	HPM Instrumentation RF Channels	Total RF Channels per HPM	FOARC Channels per HPM
NC RFQ	402.5	1		1 + 1	1 + 1	0 + 0	1 + 0	16:1 x 2	6	14
NC DTL	402.5	6		1 + 1	1 + 1	0 + 0	1 + 0	1	5	8
NC CCL	805	4		1 + 1	1 + 2	0 + 0	1 + 1	1	7	11
SRF 0.61β	805		33	1 + 1	1 + 1	1 + 1	1 + 0	0	6	5
SRF 0.81β	805		48	1 + 1	1 + 1	1 + 1	1 + 0	0	6	5
NC HEBT	805	2		1 + 1	1 + 1	0 + 0	1 + 0	1	5	8
SNS Systems		13	81							
Test Stand	402.5 & 805	1	1							
Spares	402.5	1								
Spares	805	1	6							
Total RFCS Systems		16	88							

Notes:

1. Cavity Field RF is a channel that samples the cavity RF field directly. Cavity Field IF is the precision phase- and amplitude-critical down-converted cavity field channel used by the RFCS for field and resonance control. The reference line in the tunnel provides the stable LO for the down-conversion.
2. Cavity Drive Forward and Reflected Power is the sample of the RF power at the cavity feed point.
3. RF Circulator and Splitter Load is a sample of the RF power reflected from these loads, used to detect a load failure.
4. HPM instrumentation channels are auxiliary (spare) channels provided by the HPM for monitoring RF signals of interest.
5. FOARC channels are the Fiber Optic Arc detector outputs from the High Power RF group and used by the HPM.
6. It is assumed that the requirements for the HEBT are the same as the DTL except for the operating frequency.

3 VXIbus Definition

The RFCS subsystem for each klystron is housed in a dedicated VXIbus crate. The crate contains a commercial slot zero controller (IOC), a clock distribution module (CDM), a field and resonance control function module (FRCM), a high power protect module (HPM), and a timing module. The CDM, FRCM, and HPM are all designed by LANL and use a common VXIbus interface circuit designed by Matt Stettler of LANL. The timing module (V124s) is supplied by Brookhaven National Laboratory. The general system architecture follows that which was developed on the Low Energy Demonstration Accelerator (LEDA) for the Accelerator Production of Tritium (APT) program. The LANL-designed modules are described in more detail below.

The V124s timing module transmits the system timing signals to the CDM which, in turn, passes them to the other RFCS modules. Because each V124s has more output channels than a single CDM requires, we considered using just one V124s per rack (as opposed to one per crate). This would mean that for the SRF systems, where we have two RFCS crates per rack, we would have four RF Control Systems driven by a single V124s. We rejected this option, as we did not want to have one RFCS crate dependent on timing signals originating in another. With the current arrangement, powering off a crate for module replacement or troubleshooting does not affect any neighboring systems.

Conceptual VXIbus crate layouts are shown in Figures 3-1 through 3-3. Due to the physical separation of the klystrons for the NC cavities, we will install only one RF Control system in a VXI crate for the NC systems. The SRF klystrons are located near enough to encourage savings in crate and rack count by co-locating two control systems in a single crate. This cannot be done for the NC systems because the distances between adjacent klystrons will detrimentally affect our control margin due to increased signal group delay. Hence, Figure 3-3 shows an RFCS crate to control two SRF cavities, while the NC cavities (Figures 3-1 and 3-2) have only one FRCM and HPM each (in addition to the commercial slot-zero controller (IOC), the CDM, Timing Module and Utility module). In addition, in the RFCS crate for the RFQ, there are two double-wide 16:1 solid-state RF switch modules to multiplex the RFQ signals to the HPM.

Figure 3-1. RFQ VXIbus Crate Layout

Slot	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Function	IOC	Utility Module	V124s Timing Module	CDM	FRCM		HPM	DIAGNOSTIC MUX 1		DIAGNOSTIC MUX 2				

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Figure 3-2. DTL, CCL, and HEBT VXIbus Crate Layout

Slot	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Function	IOC	Utility Module	V124s Timing Module	CDM	FRCM		HPM							

Figure 3-3. SRF VXIbus Crate Layout

Slot	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Function	IOC	Utility Module	V124s Timing Module	CDM	FRCM		HPM	FRCM		HPM				

Table 3-1. Custom LANL VXIbus Modules (Manufacturer's ID FA0₁₆)

Model Number	Device Type Register (Hex)	Module Name	Mnemonic	Drawing Number
x3914	7F4A	Field/Resonance Control Module	FRCM	155Y503006
x3915	FF4B	Clock Distribution Module	CDM	155Y503007
x3916	FF4C	HPRF Protect Module	HPM	155Y503004

Note: The first digit change from F to 7 for the FRCM defines 64k in the A24 space

3.1 Slot Zero Controller (IOC)

The standard slot zero controller (IOC) for SNS (selected by the SNS Global Controls Group) is the MVME2100 PowerPC. Specifically, we are using the MVME2100 PowerPC plus a Dawn VMEBus extender (VMEXB180D) for the SNS RF Control System. Note that this is an adapted VME slot zero controller, not a true VXIbus device. Because this is a VME card and not a true VXI module, one may not be able to simply install an off-the-shelf VXIbus instrument and expect it to work. We have shown that the MVME2100 can read/write the VXI registers and can receive interrupts; however, the complete functionality required from the P2 connector is not supported. For the LANL-designed RF Control System modules this is not an issue, but it may be one for commercial VXIbus modules.

Specifically:

- 1) Slot-based addressing doesn't work as the VME CPU doesn't handle the P2 MODID lines. In VXI one can address a board by slot number = MODID, then dynamically assign logical addresses (LA). For the RFCS, the LA is jumpered on the board, and the software can be written to configure each board's driver by just providing the LA instead of using a resource manager that tries to configure this dynamically.

- 2) The 10 MHz backplane clock generated by the slot zero module is not supported. (i.e., no CLK10+ and CLK10-)
- 3) While VXI supports 16 bit interrupt vectors, the VME CPU only switches on the lower 8 bit vector (equal to the LA). Further dispatching can happen in the interrupt service routine by reading the VXI interrupt status register which shows the higher 8 bits of the interrupt vector.

Figure 3-4. Sample VXIinfo Routine

The following is information for someone who might wish to communicate with the board via EPICS. A simple VXIInfo routine that's called with a fixed logical address works fine:

```

vxiInfo(0xb0)
    VXI Info for LA 0xB0
    ID 0x7FA0: extended device class, A16, manufacturer ID 0xFA0
    Device type 0xFF32: model code 0xF32
    Status 0101-0000-0000-1100
    Int. Control 0101-0000-0000-1100
    No A24 memory
    
```

For "resource management" all we need is the assignment of A24 base offsets for some boards that have A24 memory. This could even be handled on the vxWorks shell in the startup script.

3.2 SNS VXIbus Backplane Definition

The following (Table 3-2) depicts the ECLTRG, TTLTRG* and LBUS connections at the P2 connector on the VXIbus backplane.

Table 3-2. VXIbus Backplane Signal Assignments

Channel	Name	Source	User	Function
ECLTRG0	ADC_CLK (40MHZ)	CDM	ALL	40 MHz clock (rising edge mark)
ECLTRG1	SYNCH* (10MHZ)	CDM	ALL	10 MHz clock (rising edge mark synced to 40 MHz)
LBUS[00..11]	LBUS			Not used
TTLTRG0*	SAMPLE*	CDM	ALL	Synchronous data sample strobe. Latch data on falling edge.
TTLTRG1*	SRF_TUNE*	FRCM	HPM	SRF tuning mode fault inhibit. Orders HPM to ignore RF faults for duration of SRF_TIME during tuning of SRF cavities. Timer starts on falling edge of SRF_TUNE.
TTLTRG2*				Spare
TTLTRG3*	RF_GATE*	CDM	ALL	LOW when RF is ON / HIGH when OFF. [See Note 1]
TTLTRG4*	PREPULSE*	CDM	ALL	Sync pulse from master timing system. Falling edge is fiducial. [See Note 1]

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Channel	Name	Source	User	Function
TTLTRG5*	FAULT_L*	ALL	HPM	RF fault in LEFT half of crate. (Klystron A). LOW = FAULT (RF off)
TTLTRG6*	RF_FAULT*	FRCM HPM	MPS	Tell MPS to turn off beam during faults. LOW = FAULT (Beam off)
TTLTRG7*	FAULT_R*	ALL	HPM	RF fault in RIGHT half of crate. (Klystron B). LOW = FAULT (RF off)

Notes:

1. Timing between TTLTRG3* and TTLTRG4* is **TBD**.
2. The HPM has one hardware input (RF_PERMIT) and one hardware output (RF_FAULT*) to the machine protection system (MPS). If RF_PERMIT goes low, the HPM pulls TTLTRG5*, TTLTRG6* and TTLTRG7* low on the backplane. Likewise, if either TTLTRG5* or TTLTRG6* are asserted on the backplane, the HPM pulls RF_FAULT* output low to notify MPS of the fault. The FRCM can also pull FAULT_L* or FAULT_R* in the event that the system is in Frequency Agile mode (off frequency).

3.2.1 ECLTRG Bus Definition

Each ECL trigger is a single-ended ECL backplane line broadcast to all of the modules in the crate. The 40 MHz ADC_CLK is generated by the CDM and placed on ECLTRG0. It is received by the FRCM and the HPM to clock their analog-to-digital converters. The synchronization pulse tied to the 10 MHz reference (SYNCH*) is generated by the CDM on ECLTRG1. It is received by the FRCM and is used to synchronize the module clocks in the crate on power-up.

The FRCM generates a 20 MHz DAC_CLK on-board from the 40 MHz with a flip-flop, using the SYNCH* for its reset, forcing the DAC_CLK to have a known edge relationship with the ADC_CLK.

3.2.2 LBUS Definition

The LBUS (Local Bus) is a daisy-chained bus, having an input pin and output pin on each module on each of its lines. (The Slot-0 Controller is an exception. It only has LBUS connections on its Row C pins). The LBUS is currently not used in the RFCS, but is protected for in the FRCM and HPM designs.

3.2.3 TTLTRG* Bus Definition

The TTL trigger bus (TTLTRG*) is an open-collector, low-true bus that is accessible to all the modules in the crate, offering all of them the opportunity to receive and drive these lines. See Table 3-2, above.

The Clock Distribution Module generates a synchronous data-sampling signal (SAMPLE*) on TTLTRG0*. All the modules use this trigger to synchronously take data and latch it until read by EPICS.

The CDM puts an RF_GATE* signal onto TTLTRG3* (LOW = RF ON / HIGH= RF OFF) to indicate when the RF should be turned on. This synchronizes the pulsing of the RF carrier with the rest of the accelerator. This signal is received by the FRCM for proper field control timing, for timing its calculations of “valid” signals for resonance control, and for actually pulsing the RF drive. It is also used by the HPM as a trigger for a blanking mode (FILL_TIME) to avoid false trips due to pulse transients.

The CDM receives the PREPULSE* signal from the Timing Module and drives TTLTRG4*. This signal is picked up by the FRCM and HPM to accommodate event monitoring and timing. **This still must be better defined.**

A backplane fault signal may be generated if:

- the field errors are too large in the FRCM;
- the HPM detects an HPRF transmission system fault or receives a system fault from the MPS or EPICS RF_PERMIT input; and,
- any module that fails a built-in-test function.

These fault signals drive TTLTRG5* (FAULT_L*) or TTLTRG7* (FAULT_R*) respectively. There are two RF_FAULT* lines in order to accommodate the superconducting RF cavity systems, where there will be two RF Control systems in a single crate. The RF_FAULT* signal to the MPS may be driven by either system to notify the MPS which klystron has the fault event.

The FRCM uses these internal fault signals to keep the control loop integrator from saturating and as a trigger to stop filling the history buffers.

4 FRCM – Field / Resonance Control Module

The FRCM continuously monitors the cavity field amplitude and phase and the actual cavity resonant frequency. The field control portion of the module minimizes deviations of the cavity field amplitude and phase from their respective setpoints and compensates for the field perturbations due to the beam. The resonance control portion of the module calculates the difference between the cavity design frequency (402.5 or 805.0 MHz) and the actual cavity resonance frequency and outputs the error to EPICS. EPICS forwards this frequency error (in Hertz) to the appropriate cavity tuner system. While interrelated, these are distinct functions, both of which are accomplished by adjusting the frequency, phase, and amplitude of the RF carrier supplied to the high power transmitters. This section describes both the control strategies and the hardware approach to meet these requirements.

The SNS FRCM uses a DSP-based digital feedback/feedforward controller to regulate the field parameters of an RF cavity of the SNS LINAC. The FRCM performs feedback / feedforward control algorithms on field IF and beam RF inputs, resulting in baseband control I/Q outputs which are then up-converted to the appropriate carrier frequency prior to amplification by the High Power RF Group.

The FRCM uses two on-board Texas Instruments TMS320C62** digital signal processors (DSP). The DSPs provide the intelligence for controlling all functions of the FRCM, including the digital field feedback loop, the digital beam feedforward loop, fault monitoring, supervisory control of the analog functionality, and the VXIbus interface functions.

For the fault monitoring function, the DSP holds the control outputs in the event of an external fault, or drives the backplane fault line when the output controller saturates for a predefined time. The supervisory control of the analog circuitry allows the DSP to adjust the loop parameters based upon external commands and conditions. It includes the VXIbus interface functions such as interpreting and responding to commands in the shared A24 register-based memory.

4.1 Field Control

The FRCM maintains the cavity field at the specified magnitude and phase during normal operations by sampling the cavity field and comparing the result against a desired setpoint set *via* EPICS. There are two controllers involved in the field control strategy. One is the main P-I (Proportional-Integral) feedback controller, with a bandwidth wider than the cavity's. The other is the feed-forward controller that suppresses any repetitive noise (*e.g.*: power supply ripple) by essentially averaging over many pulses. The implementation of the feed-forward controller will be an error adaptive feed-forward controller such as an iterative learning controller (ILC). An optional beam feed-forward controller will be accommodated in the hardware but will not be implemented initially. See Tech Note LANSCE-5-TN-00-014 (LA-UR-00-4372): "SNS Superconducting Cavity Modeling - Iterative Learning Control."

4.1.1 Field Control Design and Modeling

The control algorithms for the various normal- and super-conducting cavities will be designed and modeled to assure precise control of the cavity field in compliance with the

requirements. We will use a state-space modeling program which provides linear and nonlinear functions, common signal processing and control functions, spectral stimulus/response and modern control utilities for mixed continuous and discrete-time analysis to develop and prove out the control algorithms.

Objectives of the modeling effort are to:

- Develop performance specifications for RF components and subsystems;
- Validate the system design and performance objectives;
- Optimize the control parameters and algorithms;
- Simulate the RF system under normal and transient conditions; and,
- Create a mathematical test bed for exploratory control system development.

4.2 Resonance Control

After field control, the second purpose of the FRCM is to control the resonant frequency of the accelerator cavities to maximize the RF power transfer from the klystrons to the cavities. To do this, the FRCM determines the actual resonant frequency of the cavity using an algorithm that uses both the forward power and the cavity field to calculate the imaginary part of the load admittance.

The method / algorithm in which the FRCM calculates the cavity's resonant frequency is detailed in Tech Note AOT-5-TN:008: "LLRF Technical Note on Resonance Control Algorithms." Essentially, it calculates the cavity's admittance based on the Forward and Transmitted RF signals. The imaginary part of the admittance, $\text{Im}(Y_C)$, is linear to the error of the resonant frequency of the cavity. The digital signal processor within the FRCM performs the calculation

$$\text{Im}(Y_C) = 0.2 [I_T \cdot Q_F - I_F \cdot Q_T] / [(I_F + I_R)^2 + (Q_F + Q_R)^2]$$

and outputs an error signal based on this calculation which drives the function $\text{Im}(Y_C)$ to zero (the subscript C indicates cavity, T indicates Transmitted, and F is Forward).

4.2.1 Normal Conducting Resonance Control Example

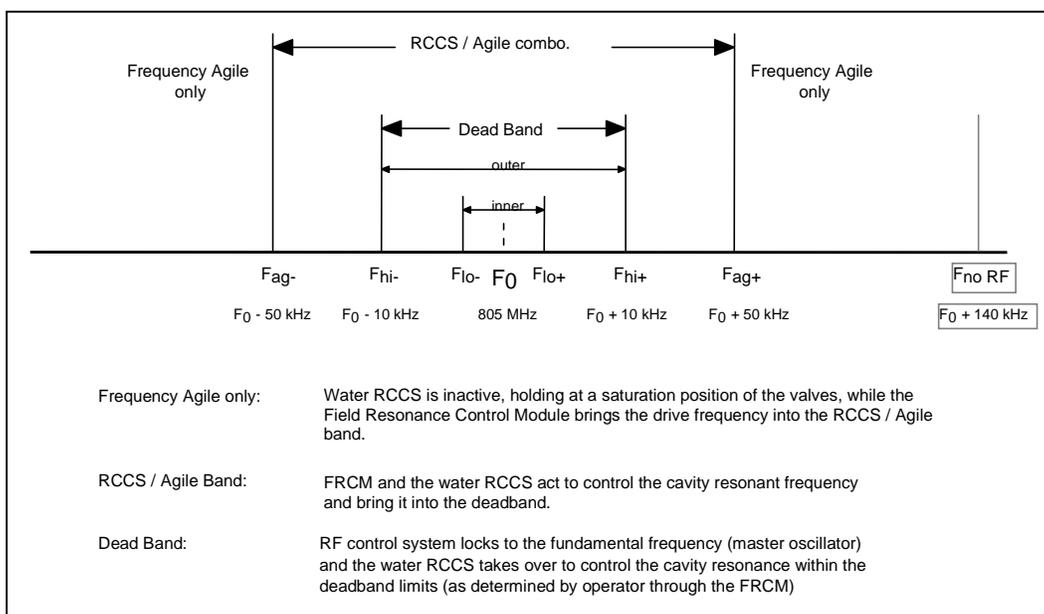
Two separate resonance control cases must be considered, normal conducting and superconducting. We will discuss use the normal-conducting (NC) cavities first. When cold, the cavities are designed to be slightly (a few hundred kHz) above their design frequency. As they heat up, they expand and their resonant frequency drops to the design point. If the cavity is far off resonance (as during a cold start) the cavity will reflect most of the RF power supplied to it if it is driven at the design frequency. Under these conditions, it makes sense to measure the cavity's actual resonant frequency and adjust the RF drive frequency to match, pumping RF power into the cavity, heating it up, and lowering its resonant frequency to the design value. We call this "Frequency Agile Mode." See Figure 4-1. Under normal operations, the typical turn-on scenario consists of turning on the klystron beam voltages, then raising the cavity field set point to the nominal value and closing the Field Control Loop. The Field Control Loop operates in Amplitude Control mode only while in the Frequency Agile mode. Once the frequency is correct, we lock to the master oscillator and the Field Control Loop automatically switches over to a full I/Q Control mode.

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The second mode occurs when the resonant frequency of the cavity is “close enough” that the Resonant Cavity Control System (RCCS) can control the cavity center frequency. Within the dead band, the FRCM locks to the design frequency and lets the RCCS control the cavity temperature (and hence, center frequency) to keep it centered at the design value. If the cavity resonant frequency moves too far off center ($F_{no\ RF}$), the RF is turned off to avoid damage to the klystrons.

The reference in the graphic to 140 kHz is cavity-specific for the CCL and CCL Hot Model. The various frequency points are adjustable *via* EPICS. Hysteresis may be implemented by specifying different cut-in and cut-out frequencies to prevent chatter at the resonance and frequency control boundary. Communication of the error frequency between the RFCS and the RCCS is accomplished through EPICS.

Figure 4-1. Frequency Agile Resonance Control



4.2.2 Superconducting Resonance Control Example

On a cold start, the RFCS must locate the resonant frequency of the superconducting cavity and force it to the design point of 805.000 MHz. It does this in a two-pass algorithm of coarse and fine frequency steps by using the frequency agile drive capability of the FRCM. The algorithm starts a number of cavity bandwidths below the 805.00 MHz design frequency and drives the cavity with approximately two seconds of RF pulses at the 60 Hz pulse repetition rate. The FRCM then increases the drive frequency by one kilohertz and repeats the process. By continuously monitoring the resulting cavity field amplitude, the FRCM can determine the coarse resonant frequency based on the cavity response – the cavity field amplitude will peak near the resonant frequency.

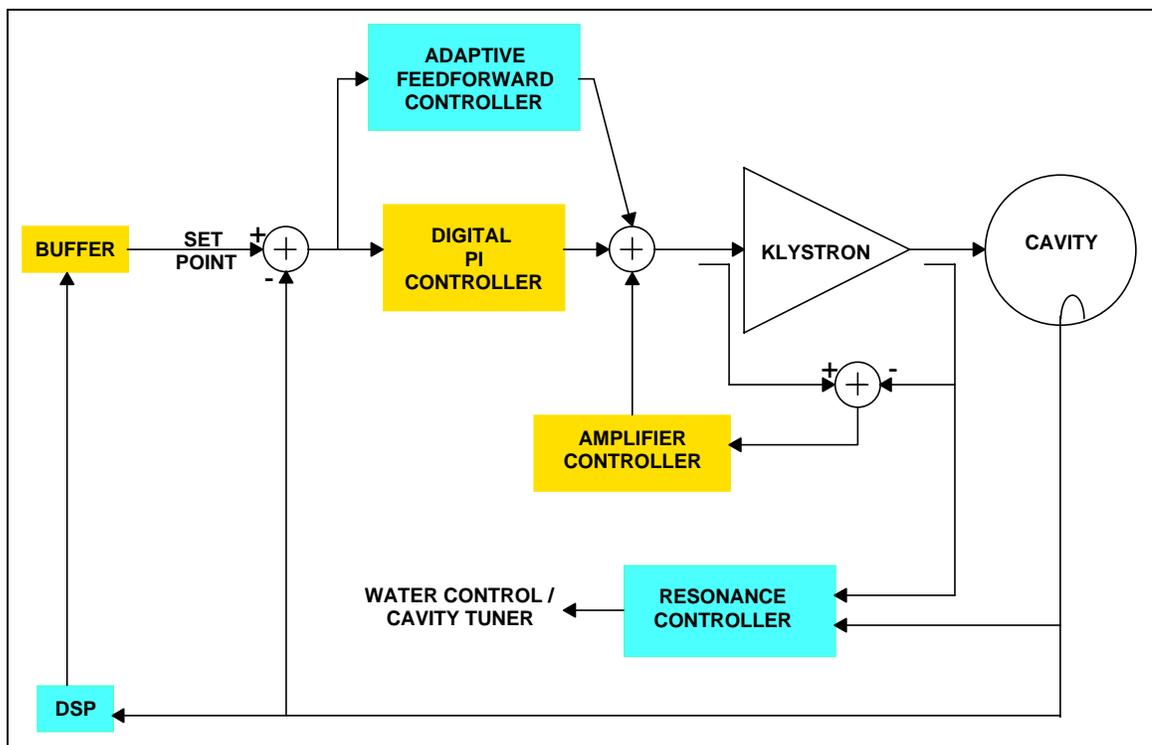
This coarse frequency then becomes the starting point for the "fine" search for the true resonant frequency. Of course, filtering will be required to help eliminate the influence of microphonics and Lorentz Force detuning. We expect that given the Q of the superconducting cavities, we can start somewhere around 805.000 MHz - 40 kHz, and step through 805 .000 MHz + 40 kHz. At two seconds per frequency, we expect this to

take approximately two minutes to locate the cavity resonant frequency. Once the actual cavity resonant frequency is found, the FRCM will send the *error frequency* (not the control signal) to the cavity tuner *via* EPICS to bring the cavity to exactly 805.000 MHz. Software (provided by others) will map the EPICS error signal from the FRCM to actual motor drive commands. During operations, the FRCM will continue to monitor the cavity resonant frequency and send an error signal to the cavity tuner as needed. Given the reputed stability of SRF cavities, this should be a relatively infrequent process.

4.3 FRCM Architecture

Figure 4-2 shows a simplified functional block diagram of the FRCM and its four major functional blocks. One is the field control, which includes a fast digital proportional-integral (P-I) controller in the main feedback control loop. The second is the amplifier controller, which regulates the Klystron output to a desired magnitude and phase determined by the main P-I feedback controller and which bandwidth will be at least one order of magnitude below the main feedback controller to prevent an instability caused by the unwanted interaction between the two controllers. The third is the feed-forward controller, which reduces repetitive noise and improves transient response during pulsed operation. The last functional block is the resonance control, which provides an error signal to maintain the RF cavity at the desired resonance frequency during normal operation and which follows the normal-conducting RF cavity resonance in the frequency agile mode during power-up and conditioning. For power-up of the superconducting RF cavities, this functional block identifies the correct resonant frequency of the cavity as well, and provides a tuner motor correction signal *via* EPICS.

Figure 4-2. FRCM Top Level Functional Block Diagram

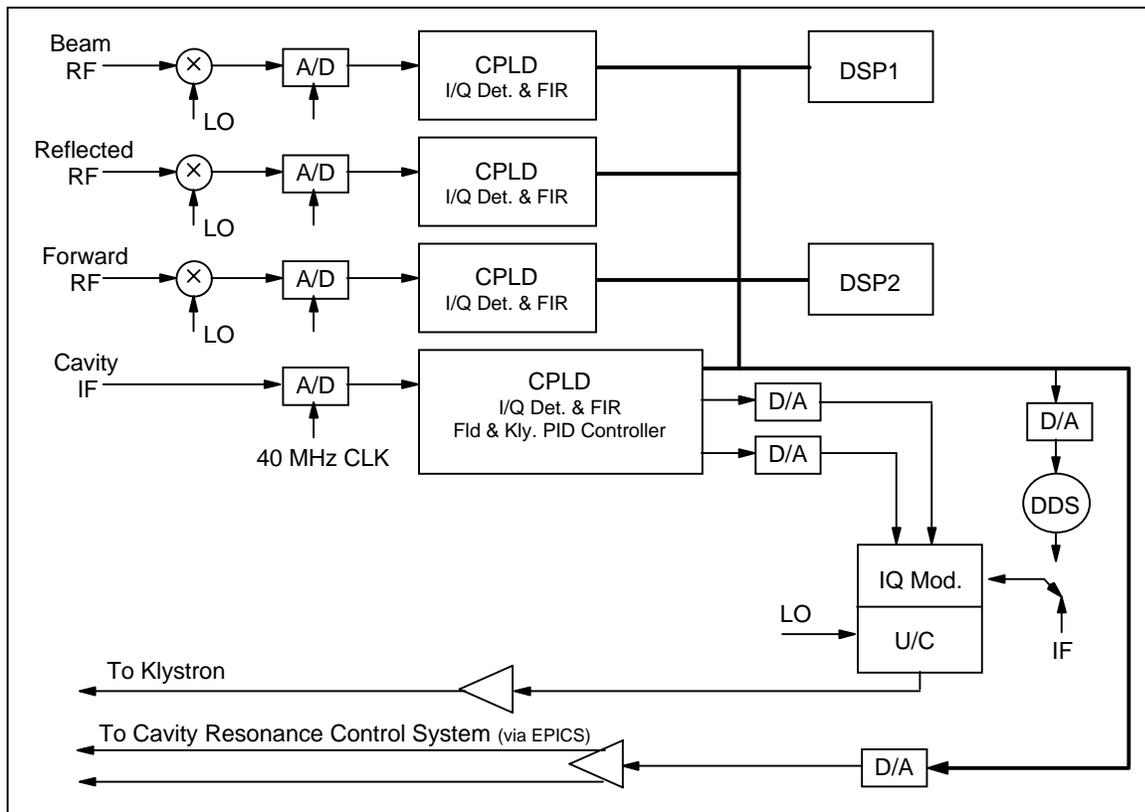


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4.3.1 FRCM Hybrid CPLD/DSP Architecture

The control algorithms are implemented by a hybrid CPLD (Complex Programmable Logic Device) / DSP based architecture in which the fast critical path signal is processed with CPLD technology for fastest throughput and minimum latency. The feed-forward and resonance control algorithms are processed through the DSPs to take full advantage of the computational power of their advanced DSP technologies. The signal flow diagram is given in Figure 4-3.

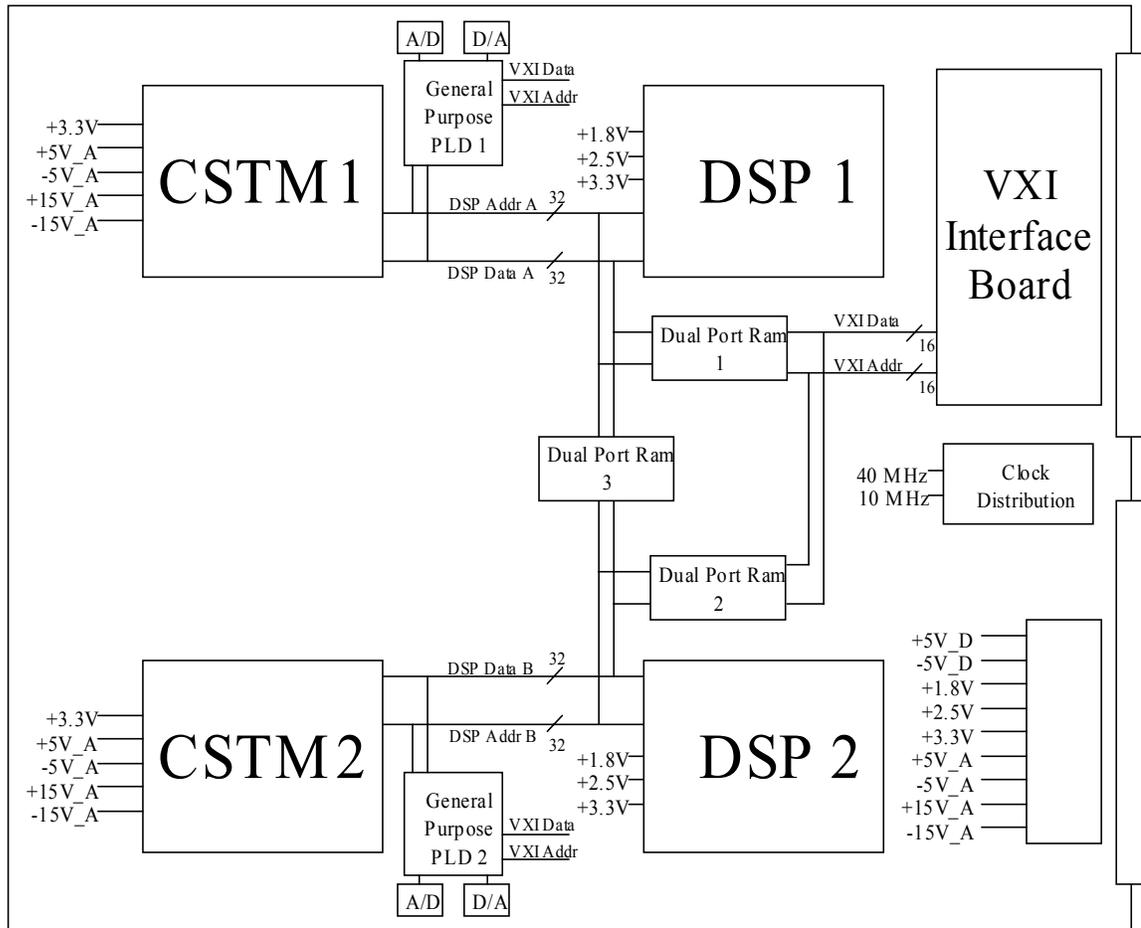
Figure 4-3. Signal Flow Diagram of the FRCM



4.4 FRCM Physical Configuration

The FRCM uses a motherboard / daughter board hardware architecture with four plug-in-board slots, two for the DSP boards and two for the front-end custom (CSTM) boards.. Figure 4-4 describes its physical layout. The motherboard provides data arbitration of the communication between the daughter boards as well as the interface with the VXI backplane, communicating with EPICS through two dual port RAMs. The inter-processor communication between the two DSPs is through Dual Port RAM 3. The detailed module I/O interface may be found in Section 4.6.3.

Figure 4-4. Physical Layout of the FRCM



4.5 FRCM Functions

4.5.1 Modes of Operation

The FRCM will be able to manage up to eight different pulse-to-pulse modes that will be defined by SNS operational requirements (e.g.: different targets, pulse widths, etc.). Note that the FRCM needs to know (via EPICS) that the previous pulse was defective or aborted so that the adaptive algorithms can reject the pulse. These modes are currently defined as:

- | | |
|---|--------|
| 0. No Pulse | 4. TBD |
| 1. Pulse 1 | 5. TBD |
| 2. Pulse 2 | 6. TBD |
| 3. Bad Pulse (e.g.: RF Fault – truncated pulse) | 7. TBD |

4.5.2 FRCM Diagnostics

FRCM diagnostics for accelerator operations are provided via the EPICS control system and over dedicated fiber optic data links to the control room. Real-time Field I and Q data for each cavity will be provided to the control room via fiber optic data links, with any

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two of the cavity fields selectable for display. The receivers for the entire LINAC's FRCM data links require about two feet of 19-inch rack space in the control room plus room for the oscilloscope to display the data. Phase and magnitude or I/Q data are available for each cavity, with filtering of the raw signals accomplished in the control room electronics.

4.5.3 RF Channel monitors

All RF and IF I/O channels have integral detector diodes for monitoring power levels which are readable through the EPICS control system.

4.5.4 Pulse Quality Monitoring:

The pulse quality is monitored and used for updating the feed-forward algorithms. The integrated power (pulse energy) is calculated for each pulse and compared to the expected value; when a pulse falls outside of the nominal bounds, the adaptive algorithms ignore the resulting data.

4.5.5 History Buffers

History buffers provide access to FRCM diagnostic data through the EPICS control system. There are nine history buffers available: Beam, Reflected, Forward, Cavity Field, Cavity Error, Uncorrected Cavity Out, Amp Error, Amp Out and Cavity Out. Any two of the six Cavity history buffers are available simultaneously. Each history buffer continuously accepts data and stops filling on the trigger event. Trigger locations are programmable at 10, 50 and 90 % of buffer capacity such that these buffers operate in the same way as a digital sampling oscilloscope, with the resolution determined by the sampling rate. The buffer length is 32K words / channel, which results in a minimum buffer length of 1.64 ms (50 ns/sample) and a maximum buffer length of 54 seconds (1.6 ms/sample).

Trigger Events

1. Fault (default) - Derived from TTLTRG bus.
2. Data/Threshold - Programmable limit for data path.
3. PREPULSE - Based on system timing.
4. Manual - Next PREPULSE after setup by EPICS.

Trigger Types

1. Single Shot (default).
2. Continuous.

Modes

1. Pulse (default). All data taken during a single pulse.
2. Period. Data taken over successive pulses.

Resolution Settings

1. High (default). Samples taken at 50 ns sampling rate.
2. Low. Samples taken at 1000 ns sample rate.
3. Programmable. Multiple of 50 ns sampling rate (1 to 32767).

4.5.6 Calibration

Each module will be calibrated prior to use to compensate for module-to-module variations in amplitude and phase response and to insure that all modules are interchangeable. This calibration corrects for module set points, component tolerances

and DC offset. *In situ* calibration of the module will provide the capability to add inter-pulse test and calibration. These features are either automatic or on-demand.

4.5.7 Built-in Self Test

The built-in self-test capability allows off-line self-stimulation to determine the full functionality of the module and its components. **NEED MORE INFO.** The FRCM motherboard will have built-in-test address and data connectors to permit testing of the CPLDs and DSPs. The interface is **TBD.**

4.6 FRCM Signal Inputs/Outputs

4.6.1 General Specifications

Digital I/Q Control:

Channel Numbers	3
Dynamic Range	60 dB
Measurement Resolution	0.01%/0.01°
Measurement Accuracy	0.1%/0.1°
Measurement Bandwidth	1 MHz
Control Bandwidth	> 200 kHz
Digital History Buffers	8x32K words

Resonance Control:

Maximum Control Bandwidth	375 kHz
Measured Frequency Accuracy	< 10 Hz
Measured Frequency Resolution	< 1 Hz
Measurement Resolution	0.01%/0.01°
Measurement Bandwidth	1 MHz
Digital History Buffers	4x32K words

Other Functionality:

Stimulus/Response characterization of control functions

4.6.2 FRCM Interface I/O

<u>Inputs:</u>	<u>Signal Level</u>	<u>Frequency</u>	<u>Connector</u>
BEAM	<10 dBm into 50 Ω	RF	PKZ
CAV_FLD	<10 dBm into 50 Ω	IF	PKZ
REF_FLD	<10 dBm into 50 Ω	RF	PKZ
FWD_FLD	<10 dBm into 50 Ω	RF	PKZ
LO	+24 dBm into 50 Ω	RF – 50 MHz	PKZ
IF	<10 dBm into 50 Ω	50 MHz	PKZ
<u>Outputs:</u>	<u>Signal Level</u>	<u>Frequency</u>	<u>Connector</u>
RF_OUT	+ 12 dBm with 50 Ω	RF	PKZ
<u>Test Points:</u>	<u>Signal Level</u>	<u>Frequency</u>	<u>Connector</u>
I	-1V to +1V into 50 Ω	DC - 5 MHz	LEMO-1
Q	-1V to +1V into 50 Ω	DC - 5 MHz	LEMO-2

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<u>LED Indicators:</u>	<u>“On” Function</u>	<u>Color</u>
MODSEL	VXIbus Address of Module	Yellow
FLD FLT	Control Saturation Fault	Red
OSC LCK	Freq. Locked to Master Oscillator	Yellow
<u>JTAG Headers:</u>	<u>Function</u>	
PLD JTAG	PLD Interface/Programming	
DSP JTAG	DSP Interface/Programming	
<u>Trigger Inputs:</u>	<u>Functionality When Driven</u>	<u>Backplane</u>
40MHz	ADC Sampling Clock	ECLTRG00
SYNCH	I/Q Synchronization Pulse	ECLTRG01
SAMPLE*	Sample I/Q Data	TTLTRG0*
RF_GATE*	RF Gate signal from CDM	TTLTRG3*
PREPULSE*	Pulse timing fiducial	TTLTRG4*
FAULT_L*	RF Fault (Left)	TTLTRG5*
FAULT_R*	RF Fault (Right)	TTLTRG7*
<u>Trigger Outputs:</u>	<u>Functionality When Driven</u>	<u>Backplane</u>
FAULT_L*	RF Shutdown Fault (Left)	TTLTRG5*
RF_FAULT*	RFCS not ready for beam	TTLTRG6*
FAULT_R*	RF Shutdown Fault (Right)	TTLTRG7*

4.6.3 FRCM VXIbus INTERFACE

<u>Configuration Registers:</u>	<u>Value</u>	<u>Bits</u>
DEVICE CLASS	Extended	01 ₂
ADDRESS SPACE	A16 / A24	00 ₂
MANUFACTURER ID	FA0 ₁₆	TBD
REQUIRED MEMORY	128k bytes	TBD
MODEL CODE	x074	TBD

<u>VXIbus Compatibility:</u>	
DEVICE CLASS	Extended Register-Based
DEVICE TYPE	Servant-only
LOGICAL ADDRESS SELECTION	Static Switch Configuration
INTERRUPTER	Programmable

4.6.4 FRCM EPICS Interface (TBD)

4.6.5 FRCM Power Requirements (TBD)

+24 VDC	-2 VDC	-24 VDC
+12 VDC	-5.2 VDC	
+5 VDC	-12 VDC	

4.7 FRCM Build Matrix TBD

5 HPM – High Power Protection Module

The HPM detects faults in the high power distribution system and interfaces the RFCS with the Machine Protection System (MPS) and the **TBD** RF_PERMIT input. For the fault detection function, it monitors the high power RF distribution system for over-threshold conditions, responds to arcs in the waveguide distribution system (FOARCs), and detects cavity arc faults. For the system interface function, it receives the hardware RF_PERMIT signal from the **TBD** system, enabling the RF carrier. In the event of a fault, it asserts the RF_FAULT* signal to the MPS, signaling the MPS to abort the beam and shut off the pulse. The various setpoints and reporting functions are accessible through EPICS. There is also an EPICS-accessible software RF_PERMIT function.

5.1 HPM Architecture

Figure 5-1. HPM Top Level Block Diagram

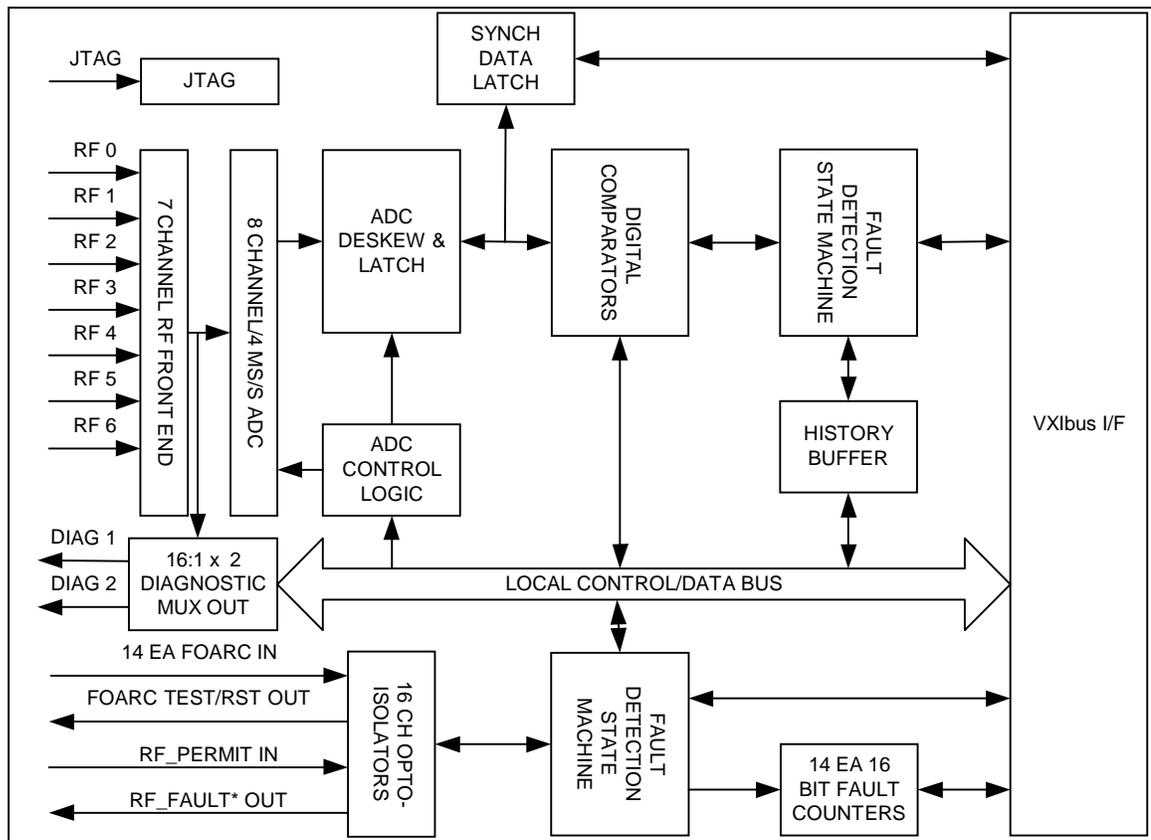


Figure 5-2 shows a simplified block diagram of the HPM. Each HPM may monitor up to seven RF channels (RF 0-6) and fourteen FOARC channels, complying with the requirements in Table 2-1. The functions of the RF channels and the FOARC channels will be considered separately. In broad terms, the RF inputs are conditioned and then sequentially digitized and de-skewed. The first seven are assigned to RF control and monitoring functions while channel 8 is a spare (not used). The data from all the analog

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channels may be latched on command from EPICS to provide a synchronous sample throughout the system and may be directed to the front panel test points through the diagnostic multiplexer.

There are three major logic blocks in the HPM (See Figure 5-1). The first is the VXIbus interface circuit designed by Matt Stettler of LANL. This proven design serves as the interface between the logic of the HPM and the VXIbus backplane and IOC. The second is the RF channel fault detection state machine. This block manages the ADC, latches, comparators, and RF fault detection logic. The third major logic block is the FOARC counters and their fault detection logic. All of the logic (with the exception of the ADC) works on a one MHz clock derived from the 40 MHz clock off the backplane. The 4 MHz ADC clock is also generated from the 40 MHz signal by division. A built-in 40 MHz clock is available in the HPM for debugging purposes, but the backplane clock should be used for normal operation.

Event counters and timers are 16 bits wide and are based on the one megahertz clock, for a maximum timer duration of 65.5 ms. It is planned that all of the logic will be accommodated in a single Altera CPLD, programmed *via* JTAG from the front panel.

5.2 HPM RF Fault Management

The HPM monitors the various RF inputs and, based on whether they are above or below a threshold, takes actions to protect the system. Two fault maturation strategies are used to improve noise immunity and to avoid nuisance trips: fill time and persistence.

The first maturation strategy is to “not look” when transients are being generated during normal operations. This is the `FILL_TIME` parameter. When the RF carrier is gated on (*via* `TTLTRG3*`), the HPM ignores any faults on all the RF (but not the FOARC) channels for the duration of `FILL_TIME`. For normal conducting cavities, it is anticipated that the `FILL_TIME` will correspond to the actual fill time of the cavities. For superconducting cavities, we expect that `FILL_TIME` will actually be shorter in duration than the SRF cavity fill time (which is 100 – 200 μ s) and will be just long enough to allow a reasonable amount of cavity field to build before enabling the RF fault trapping algorithms.

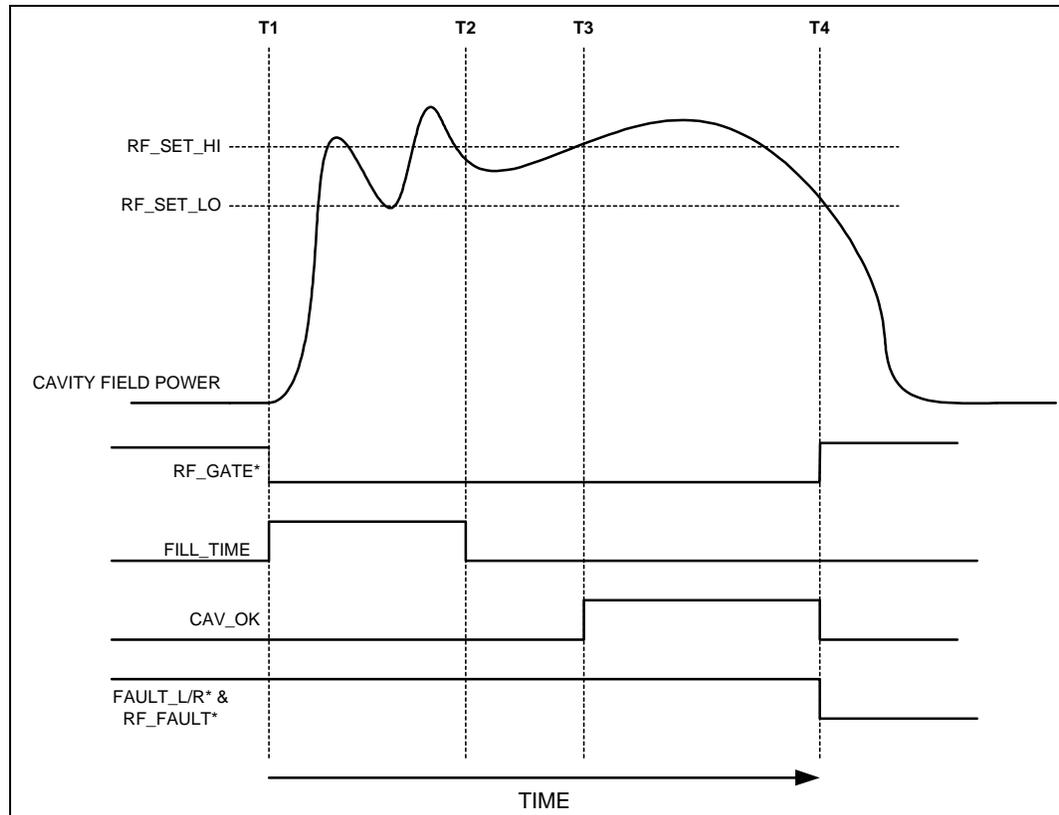
The second maturation strategy is a duration timer (*e.g.*: `RF_DLY_HI`, `RF_DLY_LO`). A timer sets a minimum time for which a fault must persist before it is matured as a fault event, discriminating against short transients. Both of these functions may be disabled by setting their durations to zero.

5.2.1 Cavity Arc Detection

The HPM monitors two kinds of RF faults: excessive RF power at the various RF waveguide test points, and arcs internal to the accelerator cavity. Detection of excessive RF power is straightforward, as it is a simple time-over-threshold function. Detection of a cavity arc is more difficult. The LEDA RFQ arc detection strategy could not distinguish between a cavity arc (causing high reflected power) and the cavity moving off resonance (causing high reflected power). If the cavity has arced, the system must shut off the RF until the arc clears; if the cavity is off resonance, the system must continue to deliver RF power to pull it back to the operating frequency (see the Frequency Agile Mode of the FRCM).

The HPM implements a cavity arc detection strategy (See Figure 5-2) suggested by Lloyd Young. This strategy monitors the RF power level in the cavity and correlates that against the RF_GATE* (TTLTRG3*) and FAULT_L/R*³ (TTLTRG5* or TTLTRG7*). Once the field is established in the cavity (rises above RF_SET_HI) and the carrier is still on (RF_GATE* is low and FAULT_L/R* is high), a drop in the field below RF_SET_LO is a clear indication of a cavity arc, signaling a fault. Hysteresis to avoid nuisance trips is provided by the gap between the upper and lower setpoints.

Figure 5-2. Cavity Arc Detection Logic



The question arises as to how to manage the startup condition. In the initial phase of gating the carrier on (T1), RF_GATE* (TTLTRG3*) goes low and the RF power in the cavity may be temporarily unstable, which would appear to be a fault condition. The solution is to add a persistence timer (FILL_TIME) at the beginning of the macropulse, triggered by the falling edge of RF_GATE*. All RF faults (but not FOARC faults) are ignored during FILL_TIME. After FILL_TIME expires (T2) and RF_GATE* is still low (OK) and RF_FAULT* is still high (OK), (meaning the RF carrier is still enabled), the cavity field must exceed the upper threshold (T3). This triggers the CAV_OK flip-flop to create a memory of the previous (good) condition. If the cavity power then drops below the lower threshold (T4), the CAV_OK flip-flop is cleared and a fault is declared, faulting RF_FAULT* to the MPS to the end of the macropulse. The times in Figure 5-1 are not to scale.

³ FAULT_L/R* is either FAULT_L* or FAULT_R* for the sake of discussion.

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5.2.2 RF Fault Actions

Once a fault has been matured and declared, the HPM blanks the RF carrier until the end of the macropulse by asserting either TTLTRG5* (FAULT_L*) or TTLTRG7* (FAULT_R*) on the backplane (selected by a klystron A / klystron B switch on the module) and notifies the MPS *via* the RF_FAULT* output. If the fault persists through the interpulse period, the fault lines are held low until it clears. Examples of possible long persistent faults are a power supply failure or a CDM PLL unlocked fault.

5.2.3 Chatter Faults

Occasionally the system will fault repeatedly on every pulse attempt – an example would be a persistent vacuum fault during conditioning or a window arcing on every pulse. These faults must be detected and the machine latched off until an operator identifies the source of the problem and restarts the machine. This function will be implemented in EPICS as an “M out of N” function, where M faulted pulses in a string of N attempts (not necessarily consecutively) will result in the machine latching off.

5.3 HPM RF Channel Inputs

5.3.1 RF Signal Processing

Each HPM card has seven identical RF processing channels consisting of a fixed attenuator, a broadband termination, and an AD8313 detector-log video amplifier. The output of the AD8313 is followed by a pair of wideband video buffer amplifiers used to adjust zero and span. The processed RF channels are multiplexed and digitized by an 8-channel - four Ms/s ADC (Exar XRD6418) for processing by the high-speed programmable logic.

Sampling eight channels (one channel is not used) at four Ms/s gives a per-channel update period of 2.0 microseconds. A channel mask (settable *via* EPICS) is available to ignore unused channels, while keeping the overall sample rate at 500 ks/s. The ADC sample latency (from the time a sample is taken to the time it appears on the digital bus) is on the order of 2.8 microseconds (TBD).

Table 5-1. General Characteristics for All HPM RF Channels

Parameter	Value
RF input power level for specified operation:	+10 to -40 dBm. Withstand power level (no damage): +20 dBm minimum
Input return loss ($F_0 \pm 5$ MHz):	12 dB minimum (<i>re</i> : 50 Ohms)
Operating Frequency:	402.5 or 805 MHz, depending on the application.
Power detection method:	Log Video Amplifier (Analog Devices AD8313)
ADC resolution:	10 bits + Overflow flag
RF Connector type:	8 Channel blind mate PKZ

5.3.2 RF Channel Power Measurement

The HPM uses an Analog Devices AD8313 detector-log-video amplifier, which means the output of the detector is equal to the logarithm of the detected signal amplitude. With appropriate scaling, this measures the RF power in the signal in dBm. The HPM detection circuits are calibrated to output $+4.95 \pm 0.01$ V with an input of +10 dBm at the front panel and $+0.95 \pm 0.01$ V with an input of -30 dBm. This scales the output of the detector to 40 dBm/4.00 V or 10 dBm/Volt. Dynamic range of the detector at the ± 1 dB uncertainty level is on the order of 60 dB (+10 dBm to -50 dBm). There are no explicit

frequency-selective components in the RF detector chain: the calibration of the HPM as a -G01 (402.5 MHz) or a -G02 (805 MHz) is to compensate for differences in the detector response at the two frequencies.

Given a ten bit (1023 count) – five Volt ADC, resolution is 4.88 mV or 0.05 dBm. ADC overflow occurs at 5.00 V or +10.5 dBm while underflow (zero count) occurs at -39.5 dBm. ADC accuracy is specified at ± 2 counts worst case or ± 0.1 dBm. If the operator displays are desired to be in Watts rather than dBm, EPICS must perform the conversion.

5.3.3 RF Channel Assignments

The RF input connector is an eight-channel blind mate PKZ by The Phoenix Company of Chicago, P/N P88P16DDF with RF channels 0-6 corresponding to connector inputs 1-7 in numerical order. Table 5-2 shows the RF channel assignments for each stage of the accelerator.

Table 5-2. HPM RF Channel Assignments

PKZ Input Number	RF Channel I	RFQ	DTL	CCL	SRF	HEBT
1	0	CAV_FLD_RF	CAV_FLD_RF	CAV_FLD_RF	CAV_FLD_RF	CAV_FLD_RF
2	1	CAV_FWD_RF	CAV_FWD_RF	CAV_FWD_RF	CAV_FWD_RF	CAV_FWD_RF
3	2	CAV_RFL_RF	CAV_RFL_RF	CAV_RFL_RF	CAV_RFL_RF	CAV_RFL_RF
4	3	CIRC_LD_RFL	CIRC_LD_RFL	CIRC_LD_RFL	CIRC_LD_RFL	CIRC_LD_RFL
5	4	MUX1_RF	CAV_PU	CAV_RFL_RF_2	KLY_FWD_RF	CAV_PU
6	5	MUX2_RF	NC	SPL_LD_RFL	KLY_RFL_RF	NC
7	6	NC	NC	CAV_PU	NC	NC
8	Not Used	N/A	N/A	N/A	N/A	N/A

5.4 HPM Fiber Optic Arc (FOARC) Detector Inputs

The HPM has fourteen FOARC inputs that are opto-isolated and diode clamped at the HPM to avoid impulse noise and ground loop problems caused by long cable runs between the HPM and the klystron controllers. The lower ten (channels 0-9) opto-isolator inputs are all returned to a common ground to the High Power RF rack, isolated from the HPM VXIbus crate ground. The grounds for the upper four may be strapped to the common ground or can be returned to a ground elsewhere in the system, adding flexibility for on/off inputs to the HPM in the future.

When an FOARC is detected (input goes LOW), the HPM turns off both the RF carrier (asserts FAULT_L/R* on the backplane) and asserts RF_FAULT* to the MPS. It holds both signals off until the end of the macropulse or until the fault clears, whichever is longer. A channel mask is provided to ignore unused FOARC channels.

The FOARC_HIST[ory] function is implemented as a 16-bit counter on each FOARC channel. Each time an FOARC is detected, its corresponding counter is incremented. These counters continue to count until reset by EPICS and may be used to generate histograms for off-line analysis. These counters are read and cleared as a block *via* EPICS and are volatile (lost on power-down of the module).

The FOARC function includes built-in-test functions (also opto-isolated) that may be activated from the control console *via* EPICS. The first is that it may assert a FOARC_TST signal to the AFT (Advanced Ferrite Technologies) FOARC chassis in the

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High Power RF rack to set all the FOARC channels. The AFT chassis must then be reset by the second control line from the HPM (FOARC_RST).

The FOARC response time (time between input line going low to RF_FAULT* going low) is **TBD**. The FOARC input connector is an AMP 747842-5 25 pin MALE right angle D-Subminiature connector. Table 5-3 shows the connector pin assignments at the HPM.

Table 5-3. HPM FOARC Connector Pin Assignments

Pin Number	Function	Pin Number	Function
1	FOARC 00 High side	15	NC
2	FOARC 01 High side	16	NC
3	FOARC 02 High side	17	+5V_REM
4	FOARC 03 High side	18	NC (GLOBAL_ARC)
5	FOARC 04 High side	19	FOARC_RST (Part of self-test)
6	FOARC 05 High side	20	FOARC_TST (Part of self-test)
7	FOARC 06 High side	21	GND_REM_1 (Primary Ground)
8	FOARC 07 High side	22	GND_REM_10 (Auxiliary Ground for FOARC 10)
9	FOARC 08 High side	23	GND_REM_11 (Auxiliary Ground for FOARC 11)
10	FOARC 09 High side	24	GND_REM_12 (Auxiliary Ground for FOARC 12)
11	FOARC 10 High side	25	GND_REM_13 (Auxiliary Ground for FOARC 13)
12	FOARC 11 High side		
13	FOARC 12 High side		
14	FOARC 13 High side		

5.5 HPM Fast Machine Control Interfaces

The high-speed interface between the RFCS and the machine control system is through a pair of opto-isolated digital channels in the HPM. **A TBD system provides the HPM with a RF_PERMIT signal (which enables, but does not turn on) the RF carrier. This system may be related to the vacuum system PLC, but its exact definition is still unknown.**

The HPM notifies the MPS of any faults in the local RFCS *via* an opto-isolated RF_FAULT* output. The interface to these two external systems at the HPM end is an AMP P/N 747840-6 9 pin MALE D-Subminiature connector. Table 5-4 shows the pin assignments for this interface at the HPM.

Table 5-4. HPM Interface Connector Pin Assignments

Pin Number	Function
1	RF_FAULT* High side (Current-limited +5V to MPS opto-isolator input)
2	Loop-back input from MPS
3	N/C
4	N/C
5	RF_PERMIT High side (Current-limited +5V to HPM opto-isolator input from TBD system)
6	RF_FAULT* Low Side (Return for MPS opto-isolator input)
7	Loop-back output to MPS
8	N/C
9	RF_PERMIT Low side (Return for HPM opto-isolator input from TBD system)

5.5.1 RF_PERMIT Input

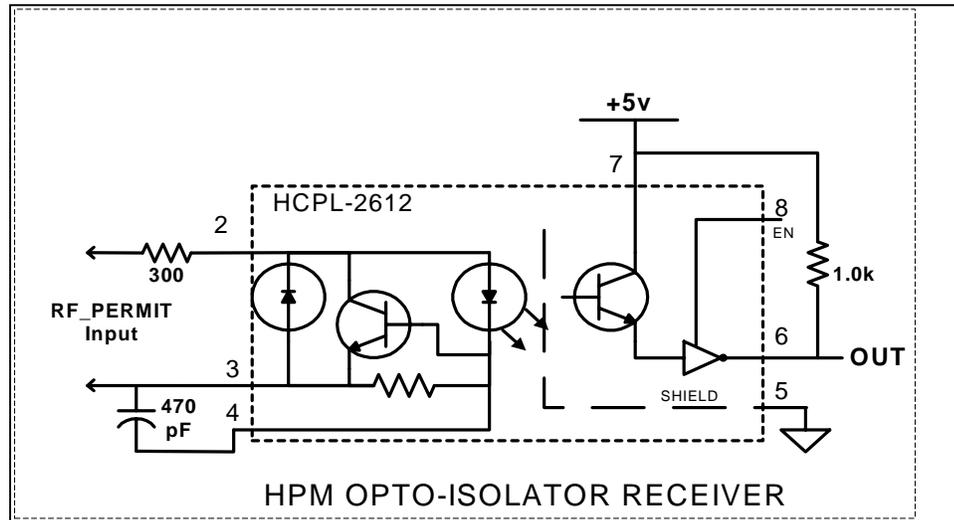
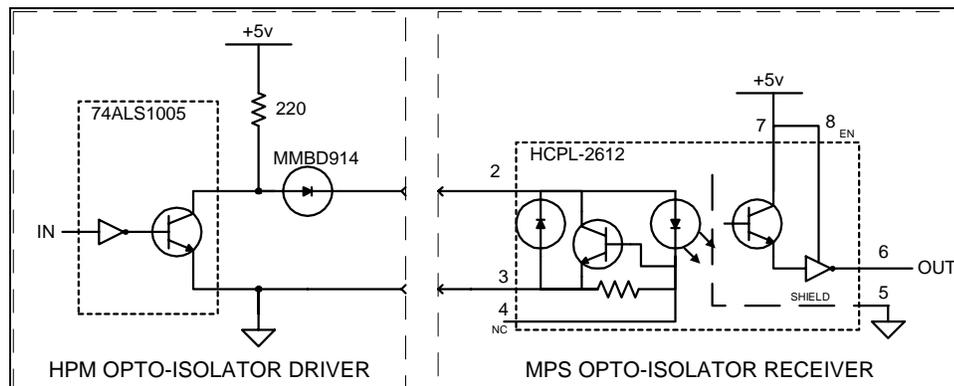


Figure 5-3. RF_PERMIT Input

The HPM provides an opto-isolated input for the RF_PERMIT signal from the **TBD** system as shown in Figure 5-3. The logic is such that a High (current into the HPM) = OK and a Low = Fault. In the event of an RF_PERMIT fault, the MPS RF_FAULT* output will be asserted for the duration of the fault. The response time (time between RF_PERMIT input line going low to RF_FAULT* going low) is **TBD**.

5.5.2 RF_FAULT* Output

Figure 5-4. RF_FAULT* Output to MPS



The HPM provides an open-collector output to drive an MPS interface module per Figure 5-4. The logic is such that a HIGH (current out of the HPM) = OK and no current out of the HPM shall indicate a fault. Note that the HPM does not read (monitor) the RF_FAULT* signal, it can only assert it. The response time (time between FAULT_L/R* going low and RF_FAULT* going low) is **TBD**.

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5.6 HPM Diagnostic Multiplexer

There is a pair of single-pin LEMO 50 Ω connectors on the front panel that allow monitoring of the various analog, FOARC, and TTLTRG* channels, selected by a pair of analog multiplexers on the board. The multiplexers are addressed *via* EPICS. The A_GND/SPARE channels are configured such that a jumper wire from anywhere on the board can be assigned to the multiplexer inputs for debugging purposes. Table 5-5 describes the diagnostic multiplexer addressing scheme.

Table 5-5. Diagnostic Multiplexer Channels

Channel Number	Mux A Function	Mux B Function
00	A_GND/SPARE	A_GND/SPARE
01	TTLTRG0*	ADC_IN0 (RF Channel 1)
02	TTLTRG1*	ADC_IN1 (RF Channel 2)
03	TTLTRG2*	ADC_IN2 (RF Channel 3)
04	TTLTRG3*	ADC_IN3 (RF Channel 4)
05	TTLTRG4*	ADC_IN4 (RF Channel 5)
06	TTLTRG5*	ADC_IN5 (RF Channel 6)
07	TTLTRG6*	ADC_IN6 (RF Channel 7)
08	TTLTRG7*	ADC_IN7 (ADC Channel 8))
09	FOARC_00	FOARC_07
10	FOARC_01	FOARC_08
11	FOARC_02	FOARC_09
12	FOARC_03	FOARC_10
13	FOARC_04	FOARC_11
14	FOARC_05	FOARC_12
15	FOARC_06	FOARC_13

5.7 HPM History Buffer

The HPM implements a **TBD k-byte** history buffer that can simultaneously monitor any two control channels as selected *via* EPICS and HISTBUFF_SRC. The contents of the history buffer are overwritten from location zero at a **TBD** rate, starting with every PREPULSE*. Data capture is accomplished by arming the acquisition with DIAG_MUX_CTL bit 15 and then triggering it *via* SAMPLE*. Once triggered, the data persist in the buffer until the bit 15 flag is cleared. Once that occurs, the data are overwritten beginning with the next PREPULSE*.

5.8 HPM Front Panel Indicators (LEDs) Normal/Fault colors

MODSEL – Yellow/black – Yellow when the HPM module is selected by the IOC.
Stretched to 20 ms for visibility.

RF_GATE – Green/black – Green when RF_GATE* (TTLTRG3*) is low (*i.e.*: RF enabled). Stretched to 20 ms for visibility.

FOARC – Green/Red – Green when the FOARC cable is connected and all inputs are high. Red if the cable is disconnected or an FOARC is received. Red stretched to 20 ms for visibility.

HP_FLT – Green/Red – Green when the HPM is NOT asserting (pulling low) the FAULT_L/R* (either TTLTRG5* or TTLTRG7*) lines on the backplane and the RF_FAULT* front panel output; red when it is. Red stretched to 20 ms for visibility.

RF_PERMIT – Green/Red – green when RF_PERMIT is high (OK) and red when it is low (faulted). Red stretched to 20 ms for visibility.

5.9 HPM Switches and Jumpers

There are three sets of on-board manual jumpers on the HPM. The first selects either the on-board 40 MHz clock oscillator for test/debug or the backplane (ECLTRG0) 40 MHz clock for normal operations. The second selects which of the fault lines on the TTLTRG* bus will be monitored and/or asserted, based on whether this module is a “lefty” or a “righty” in the crate. The third set of four jumpers allows the low side of the FOARC opto-isolators for channels 10-13 to be isolated, freeing these binary inputs for future uses in the system.

In addition to the removable jumpers, there is a set of eight soldered-in jumpers that indicate the module build/calibration level (-G01 or -G02) that is readable *via* EPICS. The two high bits (7 and 6) = 01₂ indicate a -G01 (402.5 MHz) build, while 10₂ indicates a -G02 (805 MHz) build. 00₂ and 11₂ are reserved for future releases. Bits 5 through 0 indicate the board (hardware) revision starting with 00 (original release). The firmware revision is encoded in the Altera PLD in the PLD_REV register.

5.10 HPM Front and Rear Panel Signals

<u>Front Panel Inputs:</u>	<u>Signal Level</u>	<u>Frequency</u>
FOARC Connector	Opto-TTL	100 μs PW
RF_PERMIT	Opto-TTL	N/A
RF Channels 1-7	+10 dBm Max	402.5 or 805 MHz
JTAG Program	TTL	N/A

<u>Front Panel Outputs:</u>	<u>Signal Level</u>	<u>Frequency</u>
RF_FAULT	Opto-TTL	N/A
DIAG_MUXA	Baseband Analog	<10 MHz
DIAG_MUXB	Baseband Analog	<10 MHz

<u>Backplane Inputs:</u>	<u>Functionality When Driven</u>	<u>Backplane</u>
40MHz	ADC Sampling Clock	ECLTRG0
SYNCH (10MHz)	I/Q Synchronization Pulse	ECLTRG1
SAMPLE*	Sample I/Q Data	TTLTRG0*
SRF_TUNE*	Ignore RF faults for SRF_TIME	TTLTRG1*
RF_GATE*	Carrier enable for LLRF	TTLTRG3*
PREPULSE*	RF pulse timing fiducial	TTLTRG4*
FAULT_L*	RF Shutdown Fault (Left)	TTLTRG5*
FAULT_R*	RF Shutdown Fault (Right)	TTLTRG7*

<u>Backplane Outputs:</u>	<u>Functionality When Driven</u>	<u>Backplane</u>
FAULT_L*	RF Shutdown Fault (Left)	TTLTRG5*
RF_FAULT*	RF_FAULT output to MPS	TTLTRG6*
FAULT_R*	RF Shutdown Fault (Right)	TTLTRG7*

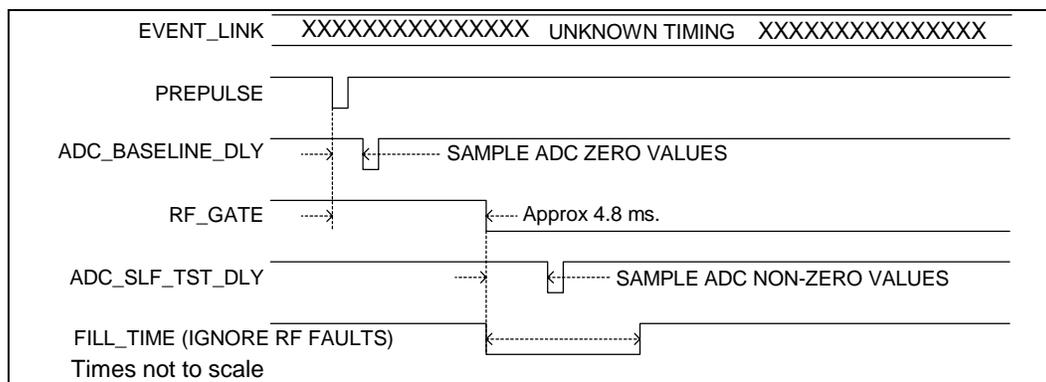
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5.11 HPM Built-In-Test (BIT) Functions

5.11.1 ADC Self Test and Accuracy Enhancement

Refer to Figure 5-5. On the falling edge of PREPULSE, the outputs of the ADC are latched after ADC_BASELINE_DLY for subtraction from the data values occurring later in the pulse. This is the zero offset voltage of the ADC. Sometime later (set by the EVENT_LINK parameters), the RF_GATE signal drops, enabling the RF carrier. The ADC_SLF_TST_DLY waits a few microseconds for the RF to come up off zero and samples the RF channels to compare them against ADC_SLF_TST_VAL. This is a diagnostic for the HPM to detect an open line or a stuck-at-zero fault; it will not detect a stuck-high channel. ADC_SLF_TST_DLY should be approximately half of FILL_TIME so that the HPM has time to switch the comparator thresholds for the BIT ADC_SLF_TST_VAL to the RF fault threshold values prior to the end of FILL_TIME. Care should be taken to avoid conflicts between this BIT function and the SAMPLE* function. Conflicts should not occur as long as SAMPLE* does not occur during FILL_TIME. Masked channels will be ignored.

Figure 5-5. Pulse Setup Timing



5.11.2 Power Supply Monitoring

The second BIT is a monitor of the power supply voltages generated on-board (High = OK). VXI crate power supplies are assumed to be monitored elsewhere. In the event of a power supply error, the module faults the RF_FAULT line to prevent improper operation.

5.11.3 Clock Monitoring

The third BIT is the detection of the 40 MHz CDM clock and the 1 and 4 MHz local timing clocks. A fault will be generated should any clock fail. For troubleshooting convenience, an on-board 40 MHz clock is provided, selectable via a jumper. The position of the jumper is readable *via* EPICS.

5.11.4 RF_FLT_TST

Asserting this EPICS function will simulate a FAULT_L/R* in the HPM, triggering the RF_FAULT output to the MPS and lighting the HP_FLT LED.

5.11.5 FOARC_TST/ FOARC_RST

Asserting FOARC_TST *via* EPICS will command the HPRF FOARC circuitry to assert the “lamp test” function in the FOARC transmitter in the High Power RF rack, faulting all the FOARC channels in the HPM. It must be followed by an FOARC_RST command to restore the FOARC transmitter to the operational state.

5.11.6 On-Board Diagnostic Connector

The HPM provides an on-board diagnostic and control connector for debugging the PLD. The pin assignments are shown in Table 5-6, below. The same connectors and pin assignments are used on FRCM motherboard.

Table 5-6. HPM Diagnostic Connector Pin Assignments

Diagnostic Data Connector- J5				Diagnostic Control Connector – J6			
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	2	GND	1	GND	2	GND
3	TEST_DATA0	4	TEST_DATA1	3	TEST_CLK	4	TEST_ENABLE
5	TEST_DATA2	6	TEST_DATA3	5	TEST_CONTROL0	6	TEST_CONTROL1
7	TEST_DATA4	8	TEST_DATA5	7	TEST_CONTROL2	8	TEST_CONTROL3
9	TEST_DATA6	10	TEST_DATA7	9	TEST_CONTROL4	10	TEST_CONTROL5
11	TEST_DATA8	12	TEST_DATA9	11	TEST_CONTROL6	12	TEST_CONTROL7
13	TEST_DATA10	14	TEST_DATA11	13		14	
15	TEST_DATA12	16	TEST_DATA13	15		16	
17	TEST_DATA14	18	TEST_DATA15	17		18	
19	TEST_DATA16	20	TEST_DATA17	19		20	
21	TEST_DATA18	22	TEST_DATA19	21		22	
23	TEST_DATA20	24	TEST_DATA21	23	TTLTRG_IN0	24	TTLTRG_IN1
25	TEST_DATA22	26	TEST_DATA23	25	TTLTRG_IN2	26	TTLTRG_IN3
27	TEST_DATA24	28	TEST_DATA25	27	TTLTRG_IN4	28	TTLTRG_IN5
29	TEST_DATA26	30	TEST_DATA27	29	TTLTRG_IN6	30	TTLTRG_IN7
31	TEST_DATA28	32	TEST_DATA29	31	TTLTRG_OUT0	32	TTLTRG_OUT1
33	TEST_DATA30	34	TEST_DATA31	33	TTLTRG_OUT2	34	TTLTRG_OUT3
35	TEST_DATA32	36	TEST_DATA33	35	TTLTRG_OUT4	36	TTLTRG_OUT5
37		38	VXI_A1	37	TTLTRG_OUT6	38	TTLTRG_OUT7
39	VXI_A2	40	VXI_A3	39	GND	40	GND
41	VXI_A4	42	VXI_A5				
43	VXI_A6	44	VXI_A7				
45	VXI_A8	46	VXI_A9				
47	VXI_A10	48	VXI_A11				
49	VXI_A12	50	VXI_A13				
51	VXI_A14	52	VXI_A15				
53	VXI_A16	54	VXI_A17				
55	VXI_A18	56	VXI_A19				
57	VXI_A20	58	VXI_A21				
59	VXI_A22	60	VXI_A23				
61	GND	62	GND				
63	VXI_D0	64	VXI_D1				
65	VXI_D2	66	VXI_D3				
67	VXI_D4	68	VXI_D5				
69	VXI_D6	70	VXI_D7				
71	VXI_D8	72	VXI_D9				
73	VXI_D10	74	VXI_D11				
75	VXI_D12	76	VXI_D13				
77	VXI_D14	78	VXI_D15				
79	GND	80	GND				

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5.12 HPM EPICS Parameters

All features and functions of the HPM (except those specifically excluded) are accessible through the VXIbus interface, accessed *via* EPICS, with the signals assigned to the user-bus (P2 Connector) corresponding to Table 3-2.

Means are provided on the HPM to assert either the TTLTRG5* (FAULT_L*) or the TTLTRG7* (FAULT_R*) lines, but not both simultaneously. Selection is *via* the left/right configuration switch internal to the module. The position of the switch is readable *via* EPICS.

The HPM implements a read-after-write and read-on-demand function for the EPICS interface for all settable parameters. Parameters are volatile (lost on power down). If power is cycled on the HPM, it will signal to EPICS that the parameter files need to be reloaded.

The EPICS signal definitions and memory map are **TBD**. Table 5-7 describes the various HPM data parameters and registers as of this document revision.

Table 5-7. HPM Data Register Descriptions⁴

EPICS Variable Name	HPM Data Register Description
ADC_BASELINE_[7..0]	Zero value of ADC channels sampled ADC_BASELINE_DLY μ s after PREPULSE (while RF is off) Bit 15 \rightarrow 11: Not used Bit 10 \rightarrow 00: ADC Data (10 bits + overflow) NORM: EPICS read only TEST: EPICS write/read
ADC_BASELINE_DLY	Time delay in μ s from falling edge of PREPULSE to latch all ADC_BASELINE_XX values while RF is off. NORM: EPICS write/read TEST: EPICS write/read
ADC_DATA_[7..0]	Time synchronized data from ADC with ADC_BASELINE_XX subtracted from it. This is the corrected data used for all HPM decisions and what is reported to EPICS. Bit 15 \rightarrow 11: Not used Bit 10 \rightarrow 00: ADC Data (10 bits + overflow) NORM: EPICS read only TEST: EPICS/Logic Analyzer read
ADC_OFL_ERR	Error byte (one bit per channel) indicating an ADC overflow error (ADC_DATA bit 10 set). Bit 15 \rightarrow 08: Not used Bit 07 \rightarrow 00: ADC Channel 7 \rightarrow 0 which overflowed. NORM: EPICS read/clear TEST: EPICS/Logic analyzer read
ADC_SAMPLE_[7..0]	Corrected ADC_DATA latched on the falling edge of SAMPLE*. Read by EPICS, overwritten by next SAMPLE* command. Bit 15 \rightarrow 11: Not used Bit 10 \rightarrow 00: ADC Data (10 bits + overflow) NORM: EPICS read TEST: EPICS write/read
ADC_SLF_TST_DLY	Time in μ s from falling edge of RF_GATE* to latch data for self-test (same for all channels). Should be less than FILL_TIME. NORM: EPICS write/read TEST: EPICS write/read

⁴ NORM: Function during normal operational modes
 TEST: Function during Built-In-Test and debug modes.

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EPICS Variable Name	HPM Data Register Description
ADC_SLF_TST_VAL_[7..0]	<p>Threshold that the SLF_TST result must exceed to be OK (may be different for each channel)</p> <p>Bit 15 → 10: Not used</p> <p>Bit 09 → 00: ADC_SLF_TST_VAL (10 bits)</p> <p>NORM: EPICS write/read</p> <p>TEST: EPICS write/read</p>
BACKPLANE	<p>Two byte flag indicating status of TTLTRG* Bus and miscellaneous data (1 = OK / 0 = FLT).</p> <p>Bit 15: DATA_REG_LOST*. Need to reload EPICS parameters.</p> <p>Bit 14: Not used</p> <p>Bit 13: Not used</p> <p>Bit 12: Not used</p> <p>Bit 11: Not used</p> <p>Bit 10: FOARC_FLT*</p> <p>Bit 09: CAV_OK (Cavity Power OK after FILL_TIME)</p> <p>Bit 08: RF_PERMIT* (Opto-isolated hardware input)</p> <p>Bit 07: TTLTRG7* (FAULT_R*)</p> <p>Bit 06: TTLTRG6* (RF_FAULT*)</p> <p>Bit 05: TTLTRG5* (FAULT_L*)</p> <p>Bit 04: TTLTRG4* (PREPULSE)</p> <p>Bit 03: TTLTRG3* (RF_GATE*)</p> <p>Bit 02: TTLTRG2* (SPARE)</p> <p>Bit 01: TTLTRG1* (SRF_TUNE*)</p> <p>Bit 00: TTLTRG0* (SAMPLE*)</p> <p>NORM: EPICS write/read</p> <p>TEST: EPICS/Logic Analyzer Write/Read</p>
CRYO_FLD_FLT1 CRYO_FLD_FLT2	Unknown functions TBD
DIAGMUX_CNTL	<p>Two byte word to control the diagnostic multiplexers. See Table 5 – 4 for channel assignments.</p> <p>Bit 15: 1 = Arm History Buffer. Trigger on SAMPLE*</p> <p>Bit 14: Not used</p> <p>Bit 13: Not used</p> <p>Bit 12: Not used</p> <p>Bit 11: Not used</p> <p>Bit 10: Not used</p> <p>Bit 09: Not used</p> <p>Bit 08: Not used</p> <p>Bit 07: DIAGMUXB_A3</p> <p>Bit 06: DIAGMUXB_A2</p> <p>Bit 05: DIAGMUXB_A1</p> <p>Bit 04: DIAGMUXB_A0</p> <p>Bit 03: DIAGMUXA_A3</p> <p>Bit 02: DIAGMUXA_A2</p> <p>Bit 01: DIAGMUXA_A1</p> <p>Bit 00: DIAGMUXA_A0</p> <p>NORM: EPICS write/read</p> <p>TEST: EPICS write/read</p>

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EPICS Variable Name	HPM Data Register Description
FAULT	<p>RF Fault word to EPICS: 1 = OK / 0 = FLT on each bit. On any HPM-generated FAULT, the IOC reads this register to determine the type of fault. This then is a pointer to the more detailed fault status registers.</p> <p>Bit 15 → 12: Not used.</p> <p>Bit 11: RF_PERMIT input failed</p> <p>Bit 10: RF Cavity Arc Fault (Computed from cavity arc algorithm)</p> <p>Bit 09: RFCS Fault Right (TTLTRG7*)</p> <p>Bit 09: MPS_OUT Fault flag (TTLTRG6*)</p> <p>Bit 08: RFCS Fault Left (TTLTRG5*)</p> <p>Bit 07: FOARC Fault</p> <p>Bit 06 → 00: Channel number of RF fault</p> <p>NORM: EPICS write/read</p> <p>TEST: EPICS/Logic Analyzer write/read</p>
FILL_TIME	<p>Duration from RF_GATE* ON (in μs) to ignore all RF FAULTS (but not FOARC faults). Same value for all RF channels in a single HPM.</p> <p>NORM: EPICS write/read</p> <p>TEST: EPICS write/read</p>
FOARC_FLT	<p>Two byte register to show which FOARC channel faulted. Cleared on next PREPULSE*.</p> <p>Bit 15: 1 = OK / 0 = One of the FOARC_HIST counters has reached FF00_h / 65280_d and is about to overflow (come read me).</p> <p>Bit 14: Not used</p> <p>Bit 13 → 00: FOARC Channel 13 → 00 faulted (Low is FAULT)</p> <p>NORM: EPICS read only</p> <p>TEST: EPICS write/read</p>
FOARC_HIST_[13..0]	<p>16 bit counter for each FOARC channel. Lost on power-down, not cleared by RST.</p> <p>NORM: EPICS read/write</p> <p>TEST: EPICS/Logic Analyzer write/read</p>
FOARC_MASK	<p>Two byte mask for FOARC channels. 1 = enable channel / 0 = ignore</p> <p>Bit 15: 1 = Set FOARC lamp test / 0 = clear (FOARC_TST)</p> <p>Bit 14: 1 = Set FOARC chassis RESET / 0 = clear (FOARC_RST)</p> <p>Bit 13 → 00: Mask to ignore FOARC Channels 13 → 00</p> <p>NORM: EPICS write/read</p> <p>TEST: EPICS/Logic Analyzer write/read</p>
HDWR_STATUS	<p>Two byte flag for HPM Hardware status. 1 = OK / 0 = fault</p> <p>Bit 15: Switch L/R status (RO): 0 = Left / 1 = Right</p> <p>Bit 14: 40 MHz Clock status (RO): 1 = External / 0 = Internal clock used</p> <p>Bit 13: +12VA_OK</p> <p>Bit 12: +5VA_OK</p> <p>Bit 11: +5VD_OK</p> <p>Bit 10: +3.3VD_OK</p> <p>Bit 09: +2.5VD_OK</p> <p>Bit 08: -2VD_OK</p> <p>Bit 07: -5.2VD_OK</p> <p>Bit 06: -12VA_OK</p> <p>Bit 05: Not used</p> <p>Bit 04: Not used</p> <p>Bit 03: Not used</p> <p>Bit 02: 1 MHz CLK OK.</p> <p>Bit 01: 4 MHz CLK OK.</p> <p>Bit 00: 40 MHz CLK OK.</p> <p>NORM: EPICS read only</p> <p>TEST: EPICS write/read</p>

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EPICS Variable Name	HPM Data Register Description																																																																																																																																																
HISTBUFF_SRC	<p>Two Byte source channel select for history buffer source data. The history buffer starts filling on each PREPULSE* and is overwritten unless triggered. The trigger is armed via DIAGMUX_CNTL bit 15. When DIAGMUX_CNTL bit 15 = 1, freeze the contents of the history buffer on the next SAMPLE*. When DIAGMUX_CNTL bit 15 = 0, resume overwriting the history buffer beginning at the next PREPULSE*.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin: 10px 0;"> <thead> <tr> <th colspan="4">Low Byte – Signal Source for Buffer A</th> <th colspan="4">High Byte – Signal Source for Buffer B</th> </tr> <tr> <th>Value</th> <th>Signal</th> <th>Value</th> <th>Signal</th> <th>Value</th> <th>Signal</th> <th>Value</th> <th>Signal</th> </tr> </thead> <tbody> <tr><td>00</td><td>TTLTRG0*</td><td>10</td><td>FOARC_00</td><td>00</td><td>TTLTRG0*</td><td>10</td><td>FOARC_00</td></tr> <tr><td>01</td><td>TTLTRG1*</td><td>11</td><td>FOARC_01</td><td>01</td><td>TTLTRG1*</td><td>11</td><td>FOARC_01</td></tr> <tr><td>02</td><td>TTLTRG2*</td><td>12</td><td>FOARC_02</td><td>02</td><td>TTLTRG2*</td><td>12</td><td>FOARC_02</td></tr> <tr><td>03</td><td>TTLTRG3*</td><td>13</td><td>FOARC_03</td><td>03</td><td>TTLTRG3*</td><td>13</td><td>FOARC_03</td></tr> <tr><td>04</td><td>TTLTRG4*</td><td>14</td><td>FOARC_04</td><td>04</td><td>TTLTRG4*</td><td>14</td><td>FOARC_04</td></tr> <tr><td>05</td><td>TTLTRG5*</td><td>15</td><td>FOARC_05</td><td>05</td><td>TTLTRG5*</td><td>15</td><td>FOARC_05</td></tr> <tr><td>06</td><td>TTLTRG6*</td><td>16</td><td>FOARC_06</td><td>06</td><td>TTLTRG6*</td><td>16</td><td>FOARC_06</td></tr> <tr><td>07</td><td>TTLTRG7*</td><td>17</td><td>FOARC_07</td><td>07</td><td>TTLTRG7*</td><td>17</td><td>FOARC_07</td></tr> <tr><td>08</td><td>ADC_IN0</td><td>18</td><td>FOARC_08</td><td>08</td><td>ADC_IN0</td><td>18</td><td>FOARC_08</td></tr> <tr><td>09</td><td>ADC_IN1</td><td>19</td><td>FOARC_09</td><td>09</td><td>ADC_IN1</td><td>19</td><td>FOARC_09</td></tr> <tr><td>0A</td><td>ADC_IN2</td><td>1A</td><td>FOARC_10</td><td>0A</td><td>ADC_IN2</td><td>1A</td><td>FOARC_10</td></tr> <tr><td>0B</td><td>ADC_IN3</td><td>1B</td><td>FOARC_11</td><td>0B</td><td>ADC_IN3</td><td>1B</td><td>FOARC_11</td></tr> <tr><td>0C</td><td>ADC_IN4</td><td>1C</td><td>FOARC_12</td><td>0C</td><td>ADC_IN4</td><td>1C</td><td>FOARC_12</td></tr> <tr><td>0D</td><td>ADC_IN5</td><td>1D</td><td>FOARC_13</td><td>0D</td><td>ADC_IN5</td><td>1D</td><td>FOARC_13</td></tr> <tr><td>0E</td><td>ADC_IN6</td><td>1E</td><td>RF_PERMIT</td><td>0E</td><td>ADC_IN6</td><td>1E</td><td>RF_PERMIT</td></tr> <tr><td>0F</td><td>ADC_IN7</td><td>1F</td><td>RF_FAULT</td><td>0F</td><td>ADC_IN7</td><td>1F</td><td>RF_FAULT</td></tr> </tbody> </table> <p>NORM: EPICS write/read TEST: EPICS/Logic Analyzer write/read</p>	Low Byte – Signal Source for Buffer A				High Byte – Signal Source for Buffer B				Value	Signal	Value	Signal	Value	Signal	Value	Signal	00	TTLTRG0*	10	FOARC_00	00	TTLTRG0*	10	FOARC_00	01	TTLTRG1*	11	FOARC_01	01	TTLTRG1*	11	FOARC_01	02	TTLTRG2*	12	FOARC_02	02	TTLTRG2*	12	FOARC_02	03	TTLTRG3*	13	FOARC_03	03	TTLTRG3*	13	FOARC_03	04	TTLTRG4*	14	FOARC_04	04	TTLTRG4*	14	FOARC_04	05	TTLTRG5*	15	FOARC_05	05	TTLTRG5*	15	FOARC_05	06	TTLTRG6*	16	FOARC_06	06	TTLTRG6*	16	FOARC_06	07	TTLTRG7*	17	FOARC_07	07	TTLTRG7*	17	FOARC_07	08	ADC_IN0	18	FOARC_08	08	ADC_IN0	18	FOARC_08	09	ADC_IN1	19	FOARC_09	09	ADC_IN1	19	FOARC_09	0A	ADC_IN2	1A	FOARC_10	0A	ADC_IN2	1A	FOARC_10	0B	ADC_IN3	1B	FOARC_11	0B	ADC_IN3	1B	FOARC_11	0C	ADC_IN4	1C	FOARC_12	0C	ADC_IN4	1C	FOARC_12	0D	ADC_IN5	1D	FOARC_13	0D	ADC_IN5	1D	FOARC_13	0E	ADC_IN6	1E	RF_PERMIT	0E	ADC_IN6	1E	RF_PERMIT	0F	ADC_IN7	1F	RF_FAULT	0F	ADC_IN7	1F	RF_FAULT
Low Byte – Signal Source for Buffer A				High Byte – Signal Source for Buffer B																																																																																																																																													
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00	TTLTRG0*	10	FOARC_00	00	TTLTRG0*	10	FOARC_00																																																																																																																																										
01	TTLTRG1*	11	FOARC_01	01	TTLTRG1*	11	FOARC_01																																																																																																																																										
02	TTLTRG2*	12	FOARC_02	02	TTLTRG2*	12	FOARC_02																																																																																																																																										
03	TTLTRG3*	13	FOARC_03	03	TTLTRG3*	13	FOARC_03																																																																																																																																										
04	TTLTRG4*	14	FOARC_04	04	TTLTRG4*	14	FOARC_04																																																																																																																																										
05	TTLTRG5*	15	FOARC_05	05	TTLTRG5*	15	FOARC_05																																																																																																																																										
06	TTLTRG6*	16	FOARC_06	06	TTLTRG6*	16	FOARC_06																																																																																																																																										
07	TTLTRG7*	17	FOARC_07	07	TTLTRG7*	17	FOARC_07																																																																																																																																										
08	ADC_IN0	18	FOARC_08	08	ADC_IN0	18	FOARC_08																																																																																																																																										
09	ADC_IN1	19	FOARC_09	09	ADC_IN1	19	FOARC_09																																																																																																																																										
0A	ADC_IN2	1A	FOARC_10	0A	ADC_IN2	1A	FOARC_10																																																																																																																																										
0B	ADC_IN3	1B	FOARC_11	0B	ADC_IN3	1B	FOARC_11																																																																																																																																										
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0F	ADC_IN7	1F	RF_FAULT	0F	ADC_IN7	1F	RF_FAULT																																																																																																																																										
LED_PW	Time in μ s that a front-panel fault LED is lit. The LED pulse stretch duration.																																																																																																																																																
PLD_REV	Revision level for PLD firmware.																																																																																																																																																
RF_DLY_HI_[7..0]	<p>Persistence (in μs) that a HI power fault must exist for (after FILL_TIME) prior to declaring a fault. Individually set for each channel.</p> <p>NORM: EPICS write/read TEST: EPICS write/read</p>																																																																																																																																																
RF_DLY_LO_[7..0]	<p>Persistence (in μs) that a LO power fault must exist for after FILL_TIME and CAV_OK prior to declaring a cavity arc fault. Used for RFQ Arc fault detect per Lloyd Young algorithm.</p> <p>NORM: EPICS write/read TEST: EPICS write/read</p>																																																																																																																																																
RF_MASK	<p>Two byte mask for RF channel enable: 1 = enable / 0 = ignore channel.</p> <p>Bit 15: RF_EN (1 = Enable RF / 0 = Disable RF) to klystron by asserting TTLTRG7* or TTLTRG5* and TTLTRG6* - Provides RF_PERMIT input for EPICS</p> <p>Bit 14: RF_FLT_TST (1 = Normal / 0 = Simulate an HPM fault on backplane and MPS)</p> <p>Bit 13 \rightarrow 08: Not used</p> <p>Bit 07 \rightarrow 00: RF channels 07 \rightarrow 00 observe / ignore faults</p> <p>NORM: EPICS write/read TEST: EPICS/Logic analyzer write/read</p>																																																																																																																																																
RF_SET_HI_[7..0]	<p>High setpoint for setting an RF Fault which persists for RF_DLY_HI μs.</p> <p>Fault = ADC_DATA_n > RF_SET_HI_n.</p> <p>NORM: EPICS write/read TEST: EPICS write/read</p>																																																																																																																																																
RF_SET_LO_[7..0]	<p>Low setpoint for calculating a cavity arc fault.</p> <p>Fault = ADC_DATA_0 < RF_SET_LO_0.</p> <p>NORM: EPICS write/read TEST: EPICS write/read</p>																																																																																																																																																
SRF_TUNE_DLY	<p>Time in μs to ignore all RF faults (but not FOARC faults) on falling edge of TTLTRG1* (SRF_TUNE*). Used during SRF tuning only.</p> <p>NORM: EPICS write/read/clear TEST: EPICS write/read/clear</p>																																																																																																																																																
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Table 5-8. HPM A16 Address Space

Base +	A16 ADDRESS [HPM Default]
00	<u>MANUFACTURER ID (RD): [CFA0_n]</u> Bit 15 → 14: Device Class [11 ₂] (Register Based) Bit 13 → 12: Address Space [00 ₂] (A16/A24) Bit 11 → 00: Manufacturer ID [FA0 _n] (LANL)
01	<u>Logical Address (WR):</u> Bit 15 → 08: Not used Bit 07 → 00: Logical Address (assigned by IOC).
02	<u>DEVICE TYPE (RD): [FF4C]</u> Bit 15 → 12: Required Memory [Depends on MSP] Bit 11 → 00: Model code [F4C] (3916 _a)
04	<u>STATUS REGISTER (RD/WR):</u> Bit 15: A24/A35 Active. Cleared on SYSRESET*, set by A24/A32 Enable bit in Control Register. Bit 14: MODID*: 1 = Device not selected / 0 = device selected. Bit 13 → 04: Device Dependant Bit 03: 1 = Ready / 0 = Register initialization failed. Bit 02: 1 = Passed Self test / 0 = Failed/busy Bit 01: Not used Bit 00: 0 = 402.5 MHz build / 1 = 805 MHz build
05	<u>CONTROL REGISTER (WR):</u> Bit 15: A24/A32 Enable: 1 = Permit, 0 = Deny Bit 14 → 02: Device Dependent (Not used) Bit 01: SYSFAIL Inhibit: 1 = Do not assert SYSFAIL*, 0 = SYSFAIL* permitted. Bit 00: Reset: 1 = Reset; 0 = Normal
06	<u>OFFSET REGISTER (RD/WR):</u> Bit 15 → 12: A24 Memory offset from bits 12→15 of DEVICE TYPE. [F]. Bit 11 → 00: Not used
07	<u>DEVICE ID REGISTER (RD):</u> Bit 06 → 15: Device Serial Number [0 to 3FFh or 1023d] Bit 00 → 05: Device revision level [0 to 3Fh or 63d]
08	<u>INTERUPT CONTROL (RD/WR):</u> Bit 15: IRQ7* Bit 14: IRQ6* Bit 13: IRQ5* Bit 12: IRQ4* Bit 11: IRQ3* Bit 10: IRQ2* Bit 09: IRQ1* Bit 08: IRQ0* (0 = IRQ) Bit 07: Interrupt Request Enable* (0 = Enable IRQ) Bit 06: Interrupt Handler Enable* (0 = Enable) Bit 05 → 03: Interrupt Request Level Bit 02 → 00: Interrupt Handler Level
0A – 3F	TBD

Notes: 1. Default values are in [].

5.13 HPM Power Requirements TBD

+24 VDC	-2 VDC	-24 VDC
+12 VDC	-5.2 VDC	
+5 VDC	-12 VDC	

5.14 HPM Build Matrix

Two versions of the HPM will be built, a -G01 and a -G02 version, differing in their calibration frequency – the physical assemblies are identical. While the -G01 version only requires a maximum of six RF channels to meet the current requirements, all seven RF channels will be stuffed in both versions to provide for future applications and to maintain commonality. Conversion from a -G01 to a -G02 and back again will merely require recalibration of the RF channel zero and span pots and a jumper change on the board to identify whether it is a -G01 or -G02 to EPICS.

Table 5-9. HPM Build Matrix

HPM Version	System Use	Frequency MHz	RF Channels Required	Total Chassis Build
G01	Breadboard & prototypes	402.5	6	5
G01	RFQ	402.5	5	1
G01	DTL	402.5	5	6
G01	Spare/Test Stand	402.5	6	2
	G01 Total Build			14
G02	Breadboard & prototypes	805	7	5
G02	CCL	805	7	4
G02	SRF – Low Beta	805	6	33
G02	SRF - High Beta	805	6	48
G02	HEBT	805	5	2
G02	Spare/Test Stand	805	7	8
	G02 Total Build			100

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6 CDM – Clock Distribution Module

The SNS Clock Distribution Module (CDM) is based on the LEDA CDM design, with the frequencies adjusted appropriately. The CDM provides synchronized clocks to the various RFCS control modules, all derived from (and phase-locked to) the 2.5 MHz reference provided from the master oscillator. The CDM design supports either one or two RF control systems in the same VXIbus crate without modification.

Physically, the CDM is a single-wide VXIbus-compliant module using both the P1 and P2 backplane connectors. RF connectors are PKZ blind mate connectors from the Phoenix Company of Chicago in D-sub housings. Test points are included on the front panel to monitor the various clock signals as well as providing a 10 MHz output which can be used as a source for synchronizing an RF generator if need be. Weight and power consumption of the module are **TBD**.

6.1 CDM Architecture

Figure 6-1. CDM Top Level Functional Block Diagram

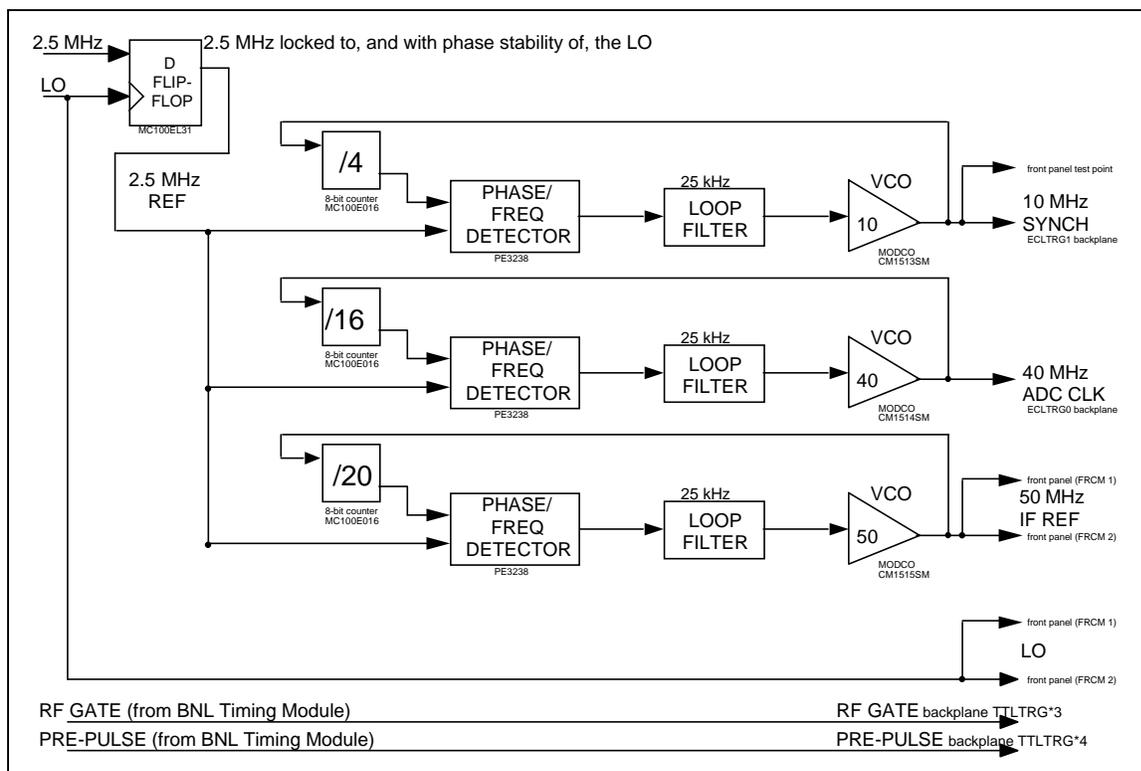


Figure 6-1 shows a simplified functional block diagram of the CDM. The CDM consists of three phase-locked loops, all tied to the 2.5 MHz REF input. This 2.5 MHz input comes from the master oscillator and is locked to the 352.5 MHz or 755 MHz LO that is distributed in the tunnel through a temperature-controlled distribution system. This LO is shipped back up to the CDM from the tunnel and is phase-locked to the 2.5 MHz signal via a D-flip-flop to insure that there is no possible phase slip between the LO and the IF

reference. For a more detailed description of the RF Reference Distribution System, see Tech Note LANSCE-5-TN-00-017 (LA-UR-00-4374): “Phase Stability Requirements for the SNS Reference Distribution System” and Chapter 7 of this document.

6.2 CDM Signal Inputs/Outputs

<u>Front Panel Inputs:</u>	<u>Signal Level</u>	<u>Connector - Frequency</u>
LO_IN	<10 dBm into 50 Ω	PKZ - 352.5 MHz or 755 MHz
REF_IN	+10 dBm into 50 Ω	PKZ - 2.5 MHz
PREPULSE*	TTL from Timing module	Lemo 50 Ω - N/A
RF_GATE*	TTL from Timing module	Lemo 50 Ω - N/A
SAMPLE*	TTL from Timing module	Lemo 50 Ω - N/A
<u>Front Panel Outputs:</u>	<u>Signal Level</u>	<u>Frequency⁵</u>
LO_OUT (x2)	+24 dBm into 50 Ω	PKZ - 352.5 MHz or 755 MHz
IF_OUT (x2)	+10 dBm into 50 Ω	PKZ - 50 MHz reference
REF_OUT	+10 dBm into 50 Ω	PKZ - 2.50 MHz reference
10_MHz	TBD dBm into 50 Ω	Lemo 50 Ω - 10.00 MHz reference test point
40_MHz	TBD dBm into 50 Ω	Lemo 50 Ω - 40.00 MHz ADC Clock test point
50_MHz	TBD dBm into 50 Ω	Lemo 50 Ω - 50.00 MHz IF test point
<u>Backplane Outputs:</u>	<u>Functionality When Driven</u>	<u>Backplane</u>
40MHz	ADC Sampling Clock	ECLTRG0
SYNCH (10MHz)	I/Q Synchronization Pulse	ECLTRG1
SAMPLE*	Sample I/Q Data	TTLTRG0*
RF_GATE*	Carrier enable for LLRF	TTLTRG3*
PREPULSE*	RF pulse timing fiducial	TTLTRG4*
FAULT_L*	RF Shutdown Fault (Left)	TTLTRG5*
FAULT_R*	RF Shutdown Fault (Right)	TTLTRG7*

Table 6-1. CDM PKZ Connector Pin Assignments

Pin	Function	Pin	Function
1	REF_IN (2.5 MHz)	5	LO_OUT_2 (352.5 or 755 MHz)
2	REF_OUT (2.5 MHz)	6	IF_OUT_1 (50 MHz)
3	LO_IN (352.5 or 755 MHz)	7	IF_OUT_2 (50 MHz)
4	LO_OUT (352.5 or 755 MHz)	8	NOT USED

⁵ CDM clock and frequency outputs are all specified to ±0.1° with respect to 50 MHz.

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6.2.1 Front Panel Indicators (LEDs) normal/fault colors:

MODSEL – Yellow – Lit when the CDM module is selected by the IOC. Stretched to 10 ms for visibility.

PLL LOCK – Green/red – red when one or more phase-locked loops is unlocked.

PWR SUPPLY – Green/Red – green when VXIbus crate external voltages are within tolerance.

6.3 CDM VXIbus INTERFACE

<u>Configuration Registers:</u>	<u>Value</u>	<u>Bits</u>
DEVICE CLASS	Extended	01 ₂
ADDRESS SPACE	A16	00 ₂
MANUFACTURER ID	4000	FA0 ₁₆
REQUIRED MEMORY	N/A	N/A
MODEL CODE	3915	F4B ₁₆

VXIbus Compatibility:

DEVICE CLASS	Extended Register-Based
DEVICE TYPE	Servant-only
LOGICAL ADDRESS SELECTION	Static Switch Configuration
INTERRUPTER	Programmable

6.4 EPICS Interface

Table 6-2 defines the CDM VXIbus A16 address space, while Table 6-3 defines the CDM status and control register.

Table 6-2. CDM A16 Address Space

OFFSET	REGISTER NAME	VALUE
00 ₁₆	LANL MANUFACTURER'S ID	7FA0 ₁₆
02 ₁₆	DEVICE TYPE	FF4B ₁₆
04 ₁₆	STATUS/CONTROL	XXXX ₁₆ see below
06 ₁₆	OFFSET	0000 ₁₆
08 ₁₆	ATTRIBUTE	XXX7 ₁₆
0A ₁₆	SERIAL NUMBER LOW	000X ₁₆
0C ₁₆	SERIAL NUMBER HIGH	0000 ₁₆
0E ₁₆	VERSION NUMBER	0000 ₁₆
10 ₁₆		BAD ₁₆
12 ₁₆		BAD ₁₆
14 ₁₆		BAD ₁₆
16 ₁₆		BAD ₁₆
18 ₁₈		BAD ₁₆
1A ₁₆		BAD ₁₆
1C ₁₆		BAD ₁₆
1E ₁₆		BAD ₁₆
20 ₁₆		BAD ₁₆
22 ₁₆		BAD ₁₆
24 ₁₆		BAD ₁₆
26 ₁₆		BAD ₁₆
28 ₁₆		BAD ₁₆
2A ₁₆		BAD ₁₆
2C ₁₆		BAD ₁₆

OFFSET	REGISTER NAME	VALUE
2E ₁₆		BAD ₁₆
30 ₁₆		BAD ₁₆
32 ₁₆		BAD ₁₆
34 ₁₆		BAD _{16s}
38 ₁₆		BAD ₁₆
3A ₁₆		BAD ₁₆
3C ₁₆		BAD ₁₆
3E ₁₆		BAD ₁₆

The CDM uses four of the status bits to tell EPICS if any of the three phase-locked loops fail, or if a power supply fails. LOW = FAIL, HIGH = OK. See Table 6-3.

Table 6-3. CDM Status Word

B15	Bit 14	B13	B12	B11-8	B7	B6	B5	B4	Bit 3	Bit 2	Bit 0-1
0	MODID*	Reserved	Prdy	Not used	PWR FAIL	10 PLL FAIL	50 PLL FAIL	40 PLL FAIL	Ready	Passed	

6.5 CDM Built-in-Test

Front panel LEDs visibly indicate the health of the module. Loop lock indicators verify that the phase-locked loops are indeed locked, and putting out power. The backplane voltages provided by the VXIbus backplane are monitored and an LED is lit should one or more of these lines fail. All of this information (excluding the loop power out) is also placed in the status/control register for communicating these conditions to the operator *via* EPICS. The Clock Distribution Module is in many ways a very "simple" module. It monitors the health of its loops at all times and flags the operator if one or more should fail.

6.6 CDM Calibration

Each module will be calibrated prior to use to compensate for module-to-module variations in amplitude and phase to insure that all modules are interchangeable to the control system.

6.7 CDM Power Requirements TBD

+24 VDC

-2 VDC

-24 VDC

+12 VDC

-5.2 VDC

+5 VDC

-12 VDC

7 Reference System

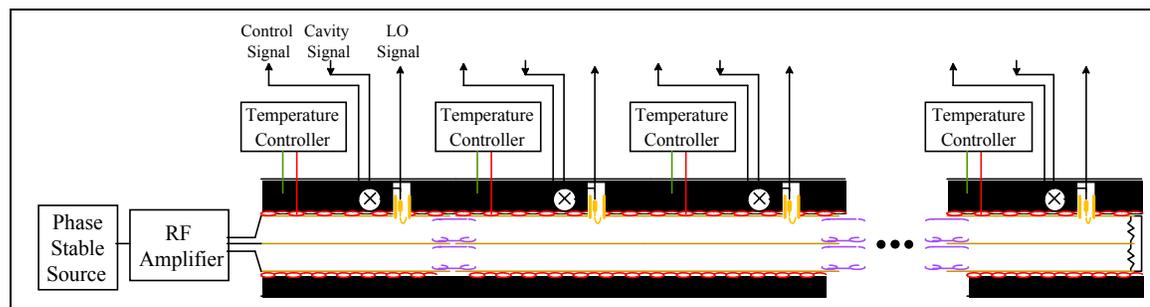
7.1 Reference System Description

The frequency reference system provides two local oscillator frequencies: 352.5 MHz (402.5 – 50) and 755 MHz (805 – 50) and a precision 2.500 MHz clock reference to the RFCS. The two LO frequencies are used to down-convert the 402.5 MHz and 805 MHz cavity signals to a 50 MHz IF in the LINAC tunnel using temperature-stabilized mixers. The resulting 50 MHz signal is brought back to the RFCS VXibus crate for digitization and processing. The 2.500 MHz signal is used as the reference for the CDMs and is synchronized to the LO frequencies at each RFCS rack.

The choice of a 50 MHz IF was based on the availability of realizable filters and commercially-available I/Q (quadrature) ADCs. The driving factor to perform the down-conversion in the tunnel is to lower the frequency of the return signal so that temperature-induced changes in the electrical length of the line will not add phase errors to the system.

Figure 7-1 shows a pictorial view of the reference frequency distribution line located in the tunnel. In it one can see the rigid coaxial line at the center with its RF slip joints, the heater strips wound around it, the RF taps, the insulation (with the cavity mixers also buried in the temperature-controlled insulation), and the Heliax runs for the LO distribution to the RFCS rack. The line is driven by a RF power amplifier and terminated in a 50-Ohm load.

Figure 7-1. Frequency Reference Line Pictorial



7.2 Reference Line Phase Stabilization

The purpose of the reference system is to provide a phase stable frequency reference at each control station. The phase of the cavity RF drive can then be set relative to the reference in order to provide the beam with the correct phase. In reality, the beam contains all of the phase information necessary to set the cavity phase but that information is not available when the beam is off, so a reference line is required.

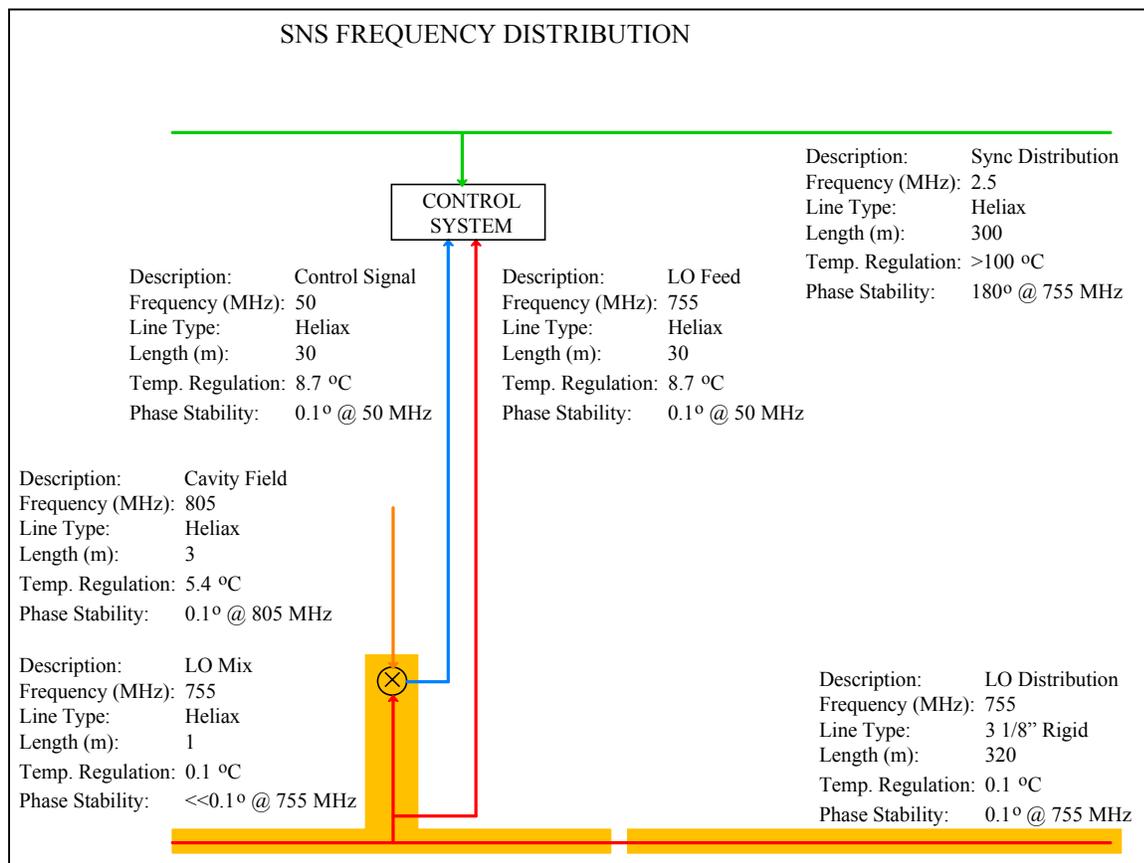
The function of the reference line is to provide a phase-stable frequency reference the length of the LINAC. To do this, the system requires a phase stable source as well as a phase stable amplifier and a phase stable distribution system. The source and amplifier will not be discussed here. The distribution system consists of a temperature-stabilized

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coaxial waveguide with taps placed at intervals corresponding to the control station locations. There are two factors in the reference distribution system that can cause an unwanted phase shift at the taps: thermal expansion/contraction of the line itself (electrical length changes), and changes in the dielectric constant of the air inside the line due to pressure variations.

Consider first the changes in physical line length due to thermal expansion, which results in an electrical length change and hence, a phase change. To minimize this effect we control the line temperature to 0.1°C . The change in length of a line with temperature is a product of the temperature change, the coefficient of thermal expansion of the material (copper), and the line length. As the total line length increases, the temperature tolerance must be smaller and smaller in order to maintain a constant phase at a given point. For the length of the SNS 755 MHz line (335 m), the temperature would have to be controlled to $\pm 20\text{ m}^{\circ}\text{C}$ in order to meet the phase specification of $\pm 0.1^{\circ}$. This is impossible. The trick is to break up the line into smaller independent units connected by slip joints. For the proposed scheme the line is broken into 100 ft (30.5 m) sections, each of which must be controlled to within $\pm 0.2^{\circ}\text{C}$. This is feasible. See Figure 7-2.

Figure 7-2. SNS Frequency Distribution Subsystem



The second source of phase error in the distribution system is variations in atmospheric pressure. These changes affect the dielectric constant of the medium (dry air), which in turn changes the propagation velocity, which then changes the phase of the wave at a given point. In order to maintain $\pm 0.1^\circ$ phase at any point the absolute pressure in the line must be regulated to ± 1 Torr.

7.3 Calculation of Reference Line Stability Requirements

The total error budget for the REF system is $\pm 0.15^\circ$ in phase at the cavity (see Table 1-2). Even though the reference system distributes two LO frequencies, 352.5 and 755 MHz, we consider only the worst-case frequency of 755 MHz. Consider the following:

At 755 MHz: $\lambda = 39.7$ cm (in vacuum) so $\pm 1.0^\circ = 1.10$ mm

For the main reference line, select Andrew part number 562A, constructed of 3 1/8" rigid copper coaxial waveguide (both inner and outer conductors) with Teflon supports for the inner conductor.

Propagation velocity: 0.998 c (air-filled)

Thermal expansion: 16.6 ppm/ $^\circ$ C

Electrical phase change in 100 ft (30.5 m) section for $\pm 1^\circ$ C temperature change: $\pm 0.46^\circ$ phase at 755 MHz (or $\pm 0.046^\circ$ phase for $\pm 0.1^\circ$ C)

Loss: 0.942 dB/100m @ 755 MHz

For the LO distribution line, select Andrew part number: LDF2-50, constructed of 3/8" flexible copper foam-filled coaxial cable.

Propagation velocity: 0.88 c

Thermal expansion: 5.6 ppm/ $^\circ$ C

Electrical phase change in 100 ft section for $\pm 1^\circ$ C temperature change:

At 755 MHz: $\pm 0.18^\circ$ phase

At 50 MHz: $\pm 0.01^\circ$ phase

We are only concerned with the phase stability of the 755 with respect to the 50 MHz because all the signal processing is tied to 50 MHz. Drift in the LO Feed phase is inside the loop and will be compensated.

For the 2.500 MHz Sync line, select Andrew LDF2-50 3/8" Helix cable. Here we avoid having to stabilize the line in temperature because the 2.500 MHz signal is re-clocked by the 755 MHz "Gold Standard" at each RFCS. As long as the 2.500 MHz does not drift by more than 180° of the 755 MHz, it will always re-synch with the 755.

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Figure 7-3. Sketch of Reference Line Installation

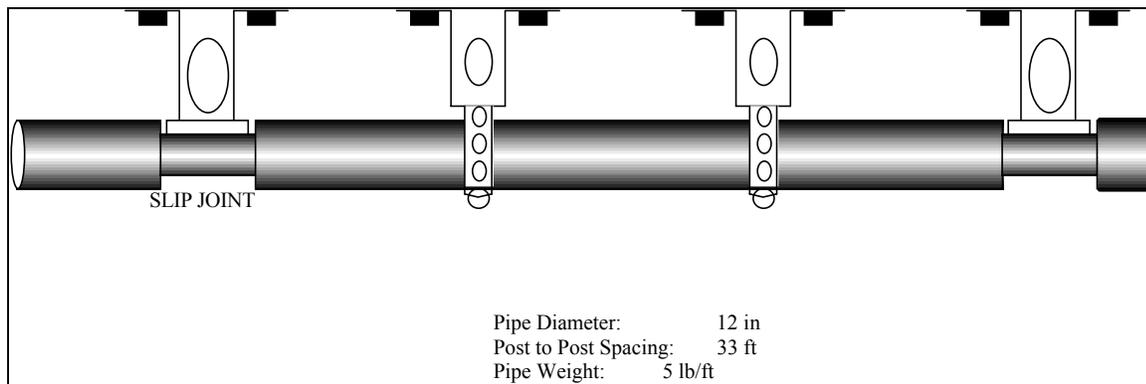


Table 7-1. Reference Line Specifications

Parameter	Specification
Frequency:	755 MHz or 352.5 MHz (depending on location)
Length:	335 m
Phase Stability:	$\pm 0.1^\circ$ @ 755 MHz
Taps	
Number of Taps:	95
Tap Power:	+21 dBm
Tap Coupling:	> 20 dB, variable in 1 dB steps
Amplifier Power:	50 Watts (+47 dBm)
Main Line	
Line Type:	3 1/8" rigid copper co-ax; pressurized with dry air
Line Lengths:	20 ft. sections with slip joints every 100 ft.
Temperature Control Method:	Electric heater and controller every 100 ft.
Temperature Control Stability:	$\pm 0.1^\circ$ C (40° C nominal temperature)
Pressure Control:	+/- 1 Torr
IF Distribution Line	
Line Type:	3/8" Heliac for LO distribution to Clock Module
Line Lengths:	100 ft. insulated and temperature controlled to $\pm 0.1^\circ$ C @ 40° C

7.4 Reference System Master Oscillator Specification

7.4.1 OUTPUT FREQUENCY

Six output frequencies are required: 2.5 MHz, 10 MHz, 452.5 MHz, 352.5 MHz, 805 MHz, and 755 MHz. All signals shall be harmonically generated from a 10 MHz crystal and phase locked to each other.

7.4.2 10 MHz CRYSTAL OSCILLATOR

The 10 MHz reference signal shall have frequency noise and stability performance equal to or better than a Wenzel Associates, Inc. Premium 10 MHz-SCULN. (SC cut crystal: stiff low noise cut. ULN: Ultra Low Noise).

7.4.3 EXTERNAL FREQUENCY REFERENCE

The source shall have the capability to be driven by an external 2.5 MHz frequency reference.

7.4.4 FREQUENCY TOLERANCE AND ADJUSTMENT

The frequency tolerance of the signals shall comply with the values of Table 7-2.

Table 7-2-- Master Oscillator Frequency Tolerance

Frequency (MHz)	Tolerance (Hz)
10	± 1
452.5	± 70
352.5	± 60
805	± 140
755	± 130
2.5	+/-0.25

(Because of the setability requirement listed below, we believe we should be able to do much better than this table).

A frequency adjustment (electronic tuning preferable) shall be available to compensate for 10 years of source aging and changes under the specified load and voltage variations (2.4). The frequency adjustment resolution of the 10 MHz signal shall be no greater than ± 0.02 Hz. The frequency adjustment range shall be equal to or greater than the frequency tolerance of the signals.

Mech. Tuning: +/- 10 Hz @ 10 MHz

Elec. Tuning: +/- 2 Hz @ 10 MHz

7.4.5 FREQUENCY STABILITY

After a 24 hour warm-up time, and within a ± 5° C window in the ambient temperature, the frequency domain stability of the signals shall comply with the values of Table 7-3.

Table 7-3. SSB Phase Noise of Frequency Source (dBc)

Offset (Hz)	2.5 MHz	10 MHz	352.5 MHz	452.5 MHz	805 MHz	755 MHz
1	≤ -117	≤ -105	≤ -74	≤ -72	≤ -67	≤ -67
10	≤ -144	≤ -132	≤ -101	≤ -99	≤ -94	≤ -94
100	≤ -154	≤ -142	≤ -111	≤ -109	≤ -104	≤ -104
1000	≤ -155	≤ -147	≤ -118	≤ -117	≤ -114	≤ -114
10000	≤ -155	≤ -147	≤ -118	≤ -117	≤ -114	≤ -114

The temperature drift shall be no more than ± 5x10⁻⁹ over the operating temperature range of 0 to 60 °C. The long-term stability shall comply with the values of Table 7-4.

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Table 7-4. Long Term Stability of Frequency Source

Time	Frequency Stability
1 day	5×10^{-10}
1 month	1.5×10^{-8}
1 year	8×10^{-9}

7.4.6 OUTPUT REQUIREMENTS

Parameter	Value
Isolation between outputs	> 80 dB
Harmonic and subharmonic signals at each frequency	< -40 dBc except 2.5 MHz < -15dbc
Non-harmonic (spurious) distortion	< -80 dBc
Source impedance	50 Ω
Frequency offset vs. load changes on each channel	< 1×10^{-10} (50 $\Omega \pm 10\%$)
Frequency offset vs. supply voltage variations on each channel	< 1×10^{-10} ($V_{CC} \pm 10\%$)
Output power at all frequencies	≥ 20 dBm except 2.5 MHz > 18dBm
Amplitude stability of outputs	1 %

7.4.7 PHASE COHERENCE

Let the phase between any of the five outputs be : $\Phi = \phi + \Delta\phi$, where the total phase difference (Φ) is the sum of a fixed phase difference (ϕ) and a time varying phase difference ($\Delta\phi$). $\Delta\phi$ must be less than $\pm 0.10^\circ$ of the higher of the two frequencies being compared, at all times. ϕ can be any value but must remain within the $\pm 0.10^\circ$ tolerance when the system power is cycled or when the internal loop slips and is re-locked.

7.4.8 INSTRUMENT STATUS INDICATORS

The instrument shall be equipped with front panel LED's that indicate power ON, the status of the phase lock loop, and any other signals that would help in diagnosing the status of the instrument.

7.4.9 PHASE TRANSIENTS

Normal laboratory vibrations shall not cause phase transients.

7.5 Reference Line Temperature Controller Interface TBD

8 Signal Technologies VXIbus 16:1 RF Multiplexer

The Signal Technologies Model 6503-001S-016S-7 is a VXIbus-compliant 16:1 solid-state RF switch rated from 50 – 1000 MHz. It is used exclusively in the RFQ section of the RFCS, where pair of them provides a 32:2 switching function for RFQ probe signals and to monitor the forward and reflected power from each of the eight RFQ feed points. It is a modification of a Signal Technologies standard product specifically developed for SNS. A description of the VMEbus interface for the switch is in an appendix.

Contact:

Tom Nelson <Tom.Nelson@sigtech.com>

Signal Technology Corporation Systems Operation

37 Sutton Road

Webster MA 01570

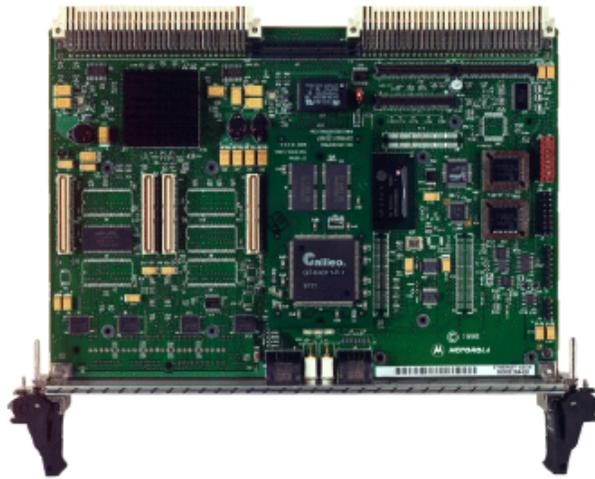
Voice: (508) 943-7440

Fax: (508) 949-1804

9 MVME2100 Power PC

MVME2100 Series

VME Processor Modules



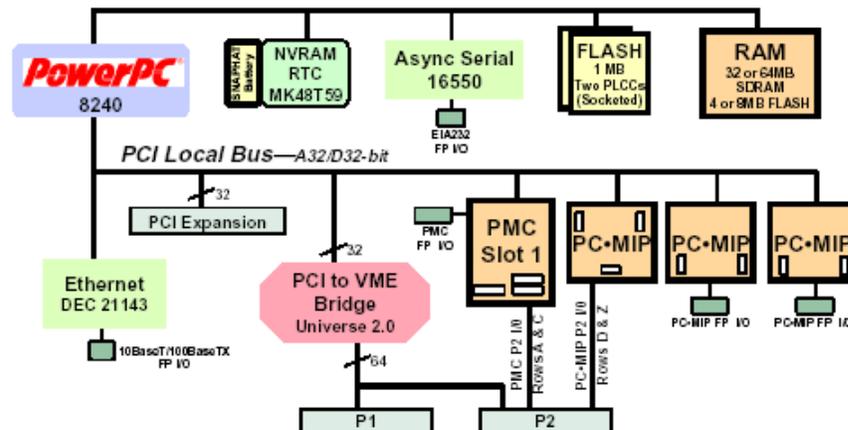
- ◆ MPC8240 32-bit microprocessor
- ◆ L1 cache—16KB/16KB PowerPC 603e™
- ◆ 32MB or 64MB of on-board SDRAM with optional ECC protection
- ◆ Two 32-pin PLCC/CLCC sockets for Flash memory; up to 1MB capacity for on-board firmware or user-specified requirements
- ◆ 4MB or 8MB on-board Flash memory for user-specified requirements
- ◆ One IEEE P1386.1 compliant 32-bit PMC slot with front-panel and P2 I/O
- ◆ Three 32-bit PC-MIP™ expansion slots, compatible with VITA 29 Draft Standard: one Type I slot with rear panel I/O and two Type II slots with front panel I/O
- ◆ 32-bit PCI expansion mezzanine connector
- ◆ Ethernet transceiver interface with 32-bit PCI local bus DMA, 10/100Mb/s with auto-negotiate speed select
- ◆ 8K x 8 NVRAM and time-of-day clock with replaceable battery backup
- ◆ Four 32-bit timers, one 16-bit timer, one watchdog timer

Modular single-board computer providing high-performance expansion I/O

The MVME2100 series of VME processor modules is a family of highly modular single-board computers for VME applications. At the heart of the MVME2100 is the MPC8240, a highly integrated PowerPC® microprocessor with a PowerPC 603e core, an advanced memory controller, and a peripheral component interconnect (PCI) interface. With the MPC8240 and a combination of PCI Mezzanine Card (PMC) and PC-MIP mezzanine slots, the MVME2100 provides customers with a high-performance building block for I/O expansion in industrial automation, telecommunications, medical, scientific, or imaging applications.



Digital DNA
from Motorola
THE HEART OF SMART.



MVME2100 Details

PC-MIP Expansion

To maximize I/O expansion flexibility, the MVME2100 features a combination of PC-MIP and PMC slots. PC-MIP is a new mezzanine standard that combines the benefits of the small form factor of IndustryPack[®] with the performance of PCI. The PC-MIP specification is in draft form before the VMEbus International Trade Association (VITA) Standards Organization as VITA 29. It is available in PDF format at VITA's standards Web page: <http://www.vita.com/vso/stds.html>.

The MVME2100 provides one Type I PC-MIP slot with rear I/O via the P2 connector and two Type II PC-MIP slots with front panel I/O. The two Type II slots can accept either one double-wide or two single-wide PC-MIP cards.

PMC Expansion

In addition to three PC-MIP slots, the MVME2100 provides one IEEE P1386.1 compliant PMC slot that supports both front panel and P2 I/O, and a mating connector to a PMC expansion mezzanine for applications requiring more real estate. A complete catalog of available off-the-shelf PMCs can be found at <http://www.groupipc.com>.

In addition to providing high-performance expansion I/O, the mezzanine slots form a common architecture for future generations of products. Changing I/O requirements can be satisfied by simply replacing the PMC or PC-MIP mezzanines

while reusing the same base platform, reducing the long-term cost of ownership.

VME64 Extension Connector

To maximize the capabilities of the MVME2100, 5-row, 160-pin DIN connectors replace the 3-row, 96-pin connectors historically used on VME for P1 and P2. Two rows, Z and D, have been added to the VME P1/J1 and P2/J2 connectors providing a user with additional I/O. The VME64 extension connector is 100% backward compatible with existing VME card systems.

Front Panel Handle Options

Part of the VME64x specification defines the use of new injector/extractor handles as defined by IEEE 1101.10. A primary benefit of this handle type is easier insertion and ejection of the VME board into and out of a backplane. Motorola offers versions of our products which are compatible with this standard.

In addition, we provide versions with the small Scanbe handles traditionally provided on VME. Consult your sales representative for part number and ordering details.

SNS RF Control System

Specifications

Processor

Microprocessor: MPC8240
 Processor Core: MPC803e
 Core Frequency: 200 MHz or 250 MHz
 External Bus Frequency: 66.67 MHz (at 200 MHz), 83 MHz (at 250 MHz)
 On-Chip Cache (L1): 16KB/16KB

Memory

Main Memory: Synchronous Dynamic RAM at 66 MHz or 83 MHz
 Capacity: 32 or 64MB
 EEPROMs: On-board, programmable
 Capacity: 1MB via two 32-pin PLCC/CLCC sockets; 4MB or 8MB surface mount
 Read Access (4-Byte port): 35 clocks at 66 MHz or 36 clocks at 83 MHz (32-byte burst)
 Read Access (1MB port): 236 clocks at 66 MHz or 268 clocks at 83 MHz (32-byte burst)
 NVRAM: 8KB; 4KB available for users
 Cell Storage Life: 50 years at 55° C
 Cell Capacity Life: 10 years at 100% duty cycle
 Removable Battery: Yes

VMEbus ANSI/VITA 1-1994 VME64 (IEEE STD 1014)

DTB Master: A16-A32; D08-D64, BLT
 DTB Slave: A24-A32; D08-D64, BLT, UAT
 Arbitrator: RR/PRI
 Interrupt Handler: IRQ 1-7/Any one of seven IRQs
 Generator:
 System Controller: Yes, jumperable or auto detect
 Location Monitor: Two, LMA32

Ethernet Interface

Controller: DEC 21143
 PCI Local bus DMA: Yes
 Connector: 10/100BaseT routed to front panel, RJ-45

Asynchronous Serial Port

Controller: PC16550
 Connector: Routed to front panel, RJ-45

Counters/Timers

TOD Clock Driver: MK8259; 8KB NVRAM
 Real-time Timers: Four, 16-bit programmable
 Counters:
 Watchdog Timer: Time-out generates reset

Miscellaneous

Front panel: Reset and Abort switches; three LEDs for Fail, Activity, SCOM

Board Size

Height: 233.4 mm (9.2 in.)
 Depth: 180.0 mm (6.3 in.)
 Front Panel Height: 261.6 mm (10.3 in.)
 Width: 19.8 mm (0.8 in.)
 Max. Component Height: 14.5 mm (0.58 in.)

Power Requirements

+5V ± 5%
 MVME2108 w/ MPC8240 @ 200 MHz: 12.5W @ 4.875-5.25V
 MVME2108 w/ MPC8240 @ 250 MHz: 15W @ 4.875-5.25V

Note: +12V and -12V power is not used on the board but is available to the PMC and PC-MIP sites.

IEEE P1386.1 PCI Mezzanine Card Slot

Address/Data: A32/D32, PMC PN1, PN2, PN4 connectors
 PCI Bus Clock: 33 MHz
 Signaling: 5V
 Power: +3.3V, +5V, ±12V, 7.5 watts maximum per PMC slot
 Physical Dimensions: 74 mm x 149 mm
 Module Types: One single-wide, front panel I/O or P2 I/O

PC-MIP Mezzanine Card Slots

Address/Data: A32/D32
 PCI Bus Clock: 33 MHz
 Signaling: 3.3V (+5V tolerant)
 Power: +3.3V, +5V, ±12V, the PC-MIP standard does not limit maximum power per slot
 Physical Dimensions: 47 mm x 90 mm
 Module Types: One Type I with P2 I/O via Rows D and Z, Two Type II with front panel I/O, support for either one double-wide or two single-wide Type II PC-MIP boards

Note: User I/O using connector P3 of the Type II PC-MIP boards is not supported.

PCI Expansion Connector

Address/Data: A32/D32
 PCI Bus Clock: 33 MHz
 Signaling: 5V
 Connector: 114-pin connector located on the planar of the MVME2100

Software Support

The MVME2100 is supported by a variety of operating systems, including a complete range of real-time operating systems and kernels.

Demonstrated MTBF

(based on a sample of eight boards in accelerated stress environment)

Mean: 190,500 hours
 95% Confidence: 107,681 hours

Safety

All printed wiring boards (PWBs) are manufactured with a flammability rating of 94V-0 by UL recognized manufacturers.

Environmental

	Operating	Nonoperating
Temperature:	0° C to +55° C, forced air cooling	-40° C to +85° C
Altitude:	5,500 m	15,000 m
Humidity (RH):	5% to 90%	5% to 90%
Vibration:	2 Gs RMS, 20-2000 Hz random	6 Gs RMS, 20-2000 Hz random

Electromagnetic Compatibility (EMC)

Intended for use in systems meeting the following regulations:

U.S.: FCC Part 15, Subpart B, Class A (non-residential)

Canada: ICES-003, Class A (non-residential)

This product was tested in a representative system to the following standards:
CE Mark per European EMC Directive 89/368/EEC with Amendments; Emissions:
EN55022 Class B; Immunity: EN55022-1

Ordering Information

Part Number	Description
MVME101-1	200 MHz MPC8240, 32MB SDRAM, 512K Flash, original VME Scambe front panel and handles
MVME101-3	200 MHz MPC8240, 32MB SDRAM, 512K Flash, IEEE 1101 compatible front panel with injector/ejector handles
MVME210-1	250 MHz MPC8240, 64MB SDRAM, 512K Flash, original VME Scambe front panel and handles
MVME210-3	250 MHz MPC8240, 64MB SDRAM, 512K Flash, IEEE 1101 compatible front panel with injector/ejector handles
Related Products	
PMCSPAN001	Primary PCI expansion, mates directly to the MVME2100 providing slots for either two single-wide or one double-wide IEEE P1386.1 compliant PMC cards, optional PMCSPAN-010, IEEE 1101 compatible front panel with injector/ejector handles
PMCSPAN001	PMCSPAN-001 with original VME Scambe front panel and handles
PMCSPAN010	Secondary PCI expansion; plugs directly into PMCSPAN-001 providing two additional PMC slots
PMCSPAN010	PMCSPAN-010 with original VME Scambe front panel and handles
MPMCxxx	Motorola's family of PMC modules; ask your sales representative for details
Documentation	
V2190A/B	MVME2100 Installation and Use Manual
V2190A/P1	MVME2100 Programmer's Reference Guide
PPCSPN001	PPCopen Installation Guide
PPCBUGA10M	PPC Bug Firmware User's Manual, Part 1 of 2
PPCBUGA20M	PPC Bug Firmware User's Manual, Part 2 of 2
PPCDAAGM	Firmware Diagnostics Manual
Documentation is available for on-line viewing and ordering at http://www.motorola.com/computerliterature	



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1-800-759-1107

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SNS RF Control System

Dawn VME P/N VMEXB180D VME-VXIbus adapter card.

Dawn Products, Inc.

47073 Warm Springs Blvd.
Fremont, CA 94539

Ph. (800) 258-DAWN
or (510) 657-4444
Fax. (510) 657-3274

10 VXIbus Crate

TBD words

Contact:

SNS RF Control System

11 Timing Module

TBD words

Contact:
Address

12 Utility Module

TBD words

Contact:

Address

SNS RF Control System

13 Appendix One – IOC Assignment Table

Shaded rows indicate a common power supply shared by multiple klystrons. Table maintained by Kay-Uwe Kasimir (LANL) as LinacRFLayOut.xls. Each Power Supply (PS) has a PLC in the PS rack. Each Transmitter has a PLC in the Transmitter rack. Updated 06/28/01.

Table 13-1. IOC Assignment Table

LINAC Section	Power Supply	Transmitter	Klystron Number	Klystron Power & Frequency	Tank/Cavity/ Klystron	HPRF IOC	Row	Rack	LLRF IOC	Row	Rack		
RFO	140 kV, 90A	1	1	2.5MW, 402.5 MHz	RFO1	HPRF_DTL1	3	CTL:DTL2 CAB01	LLRF_RFO1	1	RFC:RFO CAB01		
		2	2	2.5MW, 402.5 MHz	DTL1				LLRF_DTL1	2	RFC:DTL1 CAB01		
		3	3	2.5MW, 402.5 MHz	DTL2				LLRF_DTL2	3	RFC:DTL2 CAB01		
		4	4	2.5MW, 402.5 MHz	DTL3				LLRF_DTL3	4	RFC:DTL3 CAB01		
		5	5	2.5MW, 402.5 MHz	DTL4				LLRF_DTL4	5	RFC:DTL4 CAB01		
		6	6	2.5MW, 402.5 MHz	DTL5				LLRF_DTL5	6	RFC:DTL5 CAB01		
		7	7	2.5MW, 402.5 MHz	DTL6				LLRF_DTL6	7	RFC:DTL6 CAB01		
DTL	140 kV, 90A	1	8	5MW, 805 MHz	CCL1	HPRF_CCL1	4	CTL:CCL2 CAB02	LLRF_CCL1	2	RFC:CCL1 CAB01		
		2	9	5MW, 805 MHz	CCL2				LLRF_CCL2	5	RFC:CCL2 CAB01		
		3	10	5MW, 805 MHz	CCL3				LLRF_CCL3	6	RFC:CCL3 CAB01		
		4	11	5MW, 805 MHz	CCL4				LLRF_CCL4	8	RFC:CCL4 CAB01		
		CCL	140 kV, 90A	1	12	550kW, 805 MHz	MB1_a	HPRF_CCL2	7	CTL:CCL3 CAB02	LLRF_SC1	1	RFC:SCL1CAB01
				2	13	550kW, 805 MHz	MB1_b				LLRF_SC2	1	RFC:SCL1CAB02
				3	14	550kW, 805 MHz	MB1_c				LLRF_SC3	1	RFC:SCL1CAB03
				4	15	550kW, 805 MHz	MB2_a				LLRF_SC4	4	RFC:SCL2CAB01
SC Medium Beta	80 kV, 160A (for 6+6)	1	16	550kW, 805 MHz	MB2_b	HPRF_SC1	1	CTL:MB1 CAB01	LLRF_SC5	1	RFC:SCL1CAB01		
		2	17	550kW, 805 MHz	MB2_c				LLRF_SC6	4	RFC:SCL2CAB02		
		3	18	550kW, 805 MHz	MB3_a				LLRF_SC7	4	RFC:SCL2CAB03		
		4	19	550kW, 805 MHz	MB3_b				LLRF_SC8	4	RFC:SCL2CAB03		
		5	20	550kW, 805 MHz	MB3_c				LLRF_SC9	4	RFC:SCL2CAB02		
		6	21	550kW, 805 MHz	MB4_a				LLRF_SC10	4	RFC:SCL2CAB02		
		7	22	550kW, 805 MHz	MB4_b				LLRF_SC11	4	RFC:SCL2CAB02		
		8	23	550kW, 805 MHz	MB4_c				LLRF_SC12	4	RFC:SCL2CAB02		

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LINAC Section	Power Supply	Transmitter	Klystron Number	Klystron Power & Frequency	Tank/Cavity/ Klystron	HPRF IOC	Row	Rack	LLRF IOC	Row	Rack
SC High beta	80 kV, 160A (for 6+6)	3	24	550kW, 805 MHz	MB5_a	HPRF_SC2	6	CTL:MB5 CAB01	LLRF_SC7 (2 RFCS per IOC)	6	RFC:SCL3CAB01
			25	550kW, 805 MHz	MB5_b				LLRF_SC8 (2 RFCS per IOC)	6	RFC:SCL3CAB02
			26	550kW, 805 MHz	MB5_c				LLRF_SC9 (2 RFCS per IOC)	6	RFC:SCL3CAB03
		27	550kW, 805 MHz	MB6_a	LLRF_SC10 (2 RFCS per IOC)				9	RFC:SCL4CAB01	
		28	550kW, 805 MHz	MB6_b	LLRF_SC11 (2 RFCS per IOC)				9	RFC:SCL4CAB02	
		29	550kW, 805 MHz	MB6_c	LLRF_SC12 (2 RFCS per IOC)				9	RFC:SCL4CAB03	
		4	30	550kW, 805 MHz	MB7_a				LLRF_SC13 (2 RFCS per IOC)	10	RFC:SCL5CAB01
			31	550kW, 805 MHz	MB7_b				LLRF_SC14 (2 RFCS per IOC)	10	RFC:SCL5CAB02
			32	550kW, 805 MHz	MB7_c				LLRF_SC15 (2 RFCS per IOC)	10	RFC:SCL5CAB03
			33	550kW, 805 MHz	MB8_a				LLRF_SC16 (2 RFCS per IOC)	13	RFC:SCL6CAB01
			34	550kW, 805 MHz	MB8_b				LLRF_SC17 (2 RFCS per IOC)	13	RFC:SCL6CAB02
			35	550kW, 805 MHz	MB8_c				LLRF_SC18 (2 RFCS per IOC)	13	RFC:SCL6CAB03
	5	36	550kW, 805 MHz	MB9_a	LLRF_SC19 (2 RFCS per IOC)	15	RFC:SCL7CAB01				
		37	550kW, 805 MHz	MB9_b	LLRF_SC20 (2 RFCS per IOC)	15	RFC:SCL7CAB02				
		38	550kW, 805 MHz	MB9_c	LLRF_SC21 (2 RFCS per IOC)	15	RFC:SCL7CAB03				
		39	550kW, 805 MHz	MB10_a	LLRF_SC22 (2 RFCS per IOC)	18	RFC:SCL8CAB01				
		40	550kW, 805 MHz	MB10_b	LLRF_SC23 (2 RFCS per IOC)	18	RFC:SCL8CAB02				
		41	550kW, 805 MHz	MB10_c	LLRF_SC24 (2 RFCS per IOC)	18	RFC:SCL8CAB03				
	6	42	550kW, 805 MHz	MB11_a	LLRF_SC25 (2 RFCS per IOC)	20	RFC:SCL9CAB01				
		43	550kW, 805 MHz	MB11_b	LLRF_SC26 (2 RFCS per IOC)	20	RFC:SCL9CAB02				
		44	550kW, 805 MHz	MB11_c	LLRF_SC27	20	RFC:SCL9CAB03				
		45	550kW, 805 MHz	HB1_a							
		46	550kW, 805 MHz	HB1_b							
		47	550kW, 805 MHz	HB1_c							
	7	48	550kW, 805 MHz	HB1_d							
		49	550kW, 805 MHz	HB2_a							
		50	550kW, 805 MHz	HB2_b							
		51	550kW, 805 MHz	HB2_c							
		52	550kW, 805 MHz	HB2_d							
		53	550kW, 805 MHz	HB3_a							
	8	54	550kW, 805 MHz	HB3_b							
		55	550kW, 805 MHz	HB3_c							
		56	550kW, 805 MHz	HB3_d							
57		550kW, 805 MHz	HB4_a								
58		550kW, 805 MHz	HB4_b								
59		550kW, 805 MHz	HB4_c								
9	60	550kW, 805 MHz	HB4_d								
	61	550kW, 805 MHz	HB5_a								
	62	550kW, 805 MHz	HB5_b								
	63	550kW, 805 MHz	HB5_c								
	80 kV, 160A (for 6+5)										

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LIMAC Section	Power Supply	Transmitter	Klystron Number	Klystron Power & Frequency	Tank/Cavity/ Klystron	HPRF IOC	Row	Rack	LLRF IOC	Row	Rack
	80 kV, 160A (for 6+5)	10	64	550kW, 805 MHz	HB5_d	HPRF_SC_6	25	CTL:HB7 CAB01	(2 RFCS per IOC)		
			65	550kW, 805 MHz	HB6_a				LLRF_SC28	23	RFC:SCL10CAB01
			66	550kW, 805 MHz	HB6_b				(2 RFCS per IOC)		
			67	550kW, 805 MHz	HB6_c				LLRF_SC29	23	RFC:SCL10CAB02
			68	550kW, 805 MHz	HB6_d				(2 RFCS per IOC)		
			69	550kW, 805 MHz	HB7_a				LLRF_SC30	23	RFC:SCL10CAB03
		70	550kW, 805 MHz	HB7_b	(2 RFCS per IOC)						
		11	71	550kW, 805 MHz	HB7_c				LLRF_SC31	25	RFC:SCL11CAB01
			72	550kW, 805 MHz	HB7_d				(2 RFCS per IOC)		
			73	550kW, 805 MHz	HB8_a				LLRF_SC32	25	RFC:SCL11CAB02
			74	550kW, 805 MHz	HB8_b				(2 RFCS per IOC)		
			75	550kW, 805 MHz	HB8_c				LLRF_SC33	25	RFC:SCL11CAB03
	76		550kW, 805 MHz	HB8_d	(2 RFCS per IOC)						
	12	77	550kW, 805 MHz	HB9_a	LLRF_SC34	28	RFC:SCL12CAB01				
		78	550kW, 805 MHz	HB9_b	(2 RFCS per IOC)						
		79	550kW, 805 MHz	HB9_c	LLRF_SC35	28	RFC:SCL12CAB02				
		80	550kW, 805 MHz	HB9_d	(2 RFCS per IOC)						
		81	550kW, 805 MHz	HB10_a	LLRF_SC36	28	RFC:SCL12CAB03				
	80 kV, 160A (for 6+5)	13	82	550kW, 805 MHz	HB10_b	HPRF_SC_7	30	CTL:HB10 CAB01	LLRF_SC37	30	RFC:SCL13CAB01
			83	550kW, 805 MHz	HB10_c				(2 RFCS per IOC)		
			84	550kW, 805 MHz	HB10_d				LLRF_SC38	30	RFC:SCL13CAB02
			85	550kW, 805 MHz	HB11_a				(2 RFCS per IOC)		
			86	550kW, 805 MHz	HB11_b				LLRF_SC39	30	RFC:SCL13CAB03
87			550kW, 805 MHz	HB11_c	(2 RFCS per IOC)						
14		88	550kW, 805 MHz	HB11_d	LLRF_SC40				33	RFC:SCL14CAB01	
		89	550kW, 805 MHz	HB12_a	(2 RFCS per IOC)						
		90	550kW, 805 MHz	HB12_b	LLRF_SC41				33	RFC:SCL14CAB02	
		91	550kW, 805 MHz	HB12_c	(2 RFCS per IOC)						
		92	550kW, 805 MHz	HB12_d	LLRF_SC42				33	RFC:SCL14CAB03	
HEBT	TBD	TBD	93	5 MW, 805 MHz	HEBT1	TBD	TBD	TBD	TBD	TBD	TBD
	TBD	TBD	94	5 MW, 805 MHz	HEBT2	TBD	TBD	TBD	TBD	TBD	TBD

14 Appendix Two – Accelerator Cable Numbering

Table 14-1. Accelerator Cable Numbering Scheme

1st Digit (per Cabling SRD)	
No.	
1	Unassigned
2	Personnel Protection System (PPS) & Target Protection System (TPS)
3	Front End Systems
4	Linac Systems (cold and warm)
5	Ring and Transfer Line Systems
6	Target Systems (including dumps)
7	Instruments
8	Conventional Facilities
9	Integrated Controls Systems

2nd Digit				
No.	Front End and Linac	Ring & Transfer Lines	PPS/TPS	Integrated Control Sys
1	RF Power	RF Power and Controls	PPS	Network backbone cabling
2	RF Controls	Extraction Kicker	PPS	Network drops to IOCs
3	Cryogenics	Magnet HEBT	PPS	Network drops to FE PLCs
4	Cooling water sys	Magnet RTBT	PPS	Network drops to Linac PLCs
5	Magnet Linac	Magnet Ring	PPS	Network drops to Ring PLCs
6	Diagnostics	Diagnostics	TPS	Network drops to Tgt PLCs
7	Vacuum	Vacuum	TPS	Network drops to Cryo PLCs
8	Miscellaneous	Miscellaneous	TPS	Network drops to CF PLCs
9	Controls	Controls	TPS	Network drops to PPS PLCs

2nd Digit Definitions	
RF	RF power for the Linac, RF power and controls for the Ring
RF Controls	Low Level RF controls for the Linac
Magnet Linac	Power & controls signals
Magnet HEBT	Power & controls signals
Magnet RTBT	Power & controls signals
Magnet Ring	Power & controls signals
Extraction Kicker	Extraction Kicker and PFN cabling
Diagnostics	All cabling in beam diagnostics systems
Vacuum	Power & controls signals
Cooling water systems	Power & controls signals
Cryogenics	Power & controls signals
Miscellaneous	Unassigned numbers to be used as needed
Controls	Controls signals not included in areas above

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3rd Digit		
No.	Front End and Linac	Ring & Transfer Lines (1)
A	Ions Source	
B	RFQ	
C	LEBT	
D	MEBT	
E	DTL	
F	CCL	
G	MB SCL	
H	HB SCL	
J	SC warm sect's	
K	CHL	
L		HEBT
M		Ring
N		RTBT
1		VLLS - diagnostics and other very low level signals
2		LLS - low level signal and communications
3		120 - 480VAC Power
4		< 600 VDC magnet and other power
5		> 600 VDC pulse and other power
6		> 600 VAC Power
7		RF Power
8		Unassigned
9		Ground

Table data courtesy of John Cleaves, ORNL dated 06/25/01.

SNS RF Control System

Table 14-2. Cable Numbering Responsibilities

1st	2nd	3rd	System, Subsystem, or Area	Lab	Person
1			Not assigned		Les Ottinger
2			Personnel & Target Protection systems (PPS)/(TPS)	SNS	
	1-5		PPS		Paul Wright
	6-9		TPS		Ron Battle
3			Front End Systems (1)	LBNL	Bill Abraham
	1		RF	LBNL	Bill Abraham
	2		RF Controls	LBNL	Bill Abraham
	3		Cryogenics	LBNL	Bill Abraham
	4		Cooling water sys	LBNL	Bill Abraham, Steve Lewis
	5		Magnet Linac	LBNL	Bill Abraham
	6		Diagnostics	LBNL	Bill Abraham
	7		Vacuum	LBNL	Bill Abraham, Steve Lewis
	8		Miscellaneous	LBNL	Bill Abraham
	9		Controls	LBNL	Steve Lewis
4			Linac Systems (1)	LANL	Jack Gioia
	1		RF	LANL	Paul Tallerico
	2		RF Controls	LANL	Amy Reagan
	3		Cryogenics	LANL	
	4		Cooling water sys		
		E,F	DTL & CCL	LANL	John Bernardin, Bob Dalesio
		G-K	MB, HB, CHL, & Warm Sections	JLAB	John Hogan, Herb Strong
	5		Magnet Linac	LANL	Jack Gioia
	6		Diagnostics	LANL	Mike Plum
	7		Vacuum		
		E,F	DTL & CCL	LANL	John Bernardin, Bob Dalesio
		G-K	MB, HB, CHL, & Warm Sections	JLAB	John Hogan, Herb Strong
	8		Miscellaneous	LANL	Jack Gioia
	9		Controls		
		E,F	DTL & CCL	LANL	Bob Dalesio
		G-K	MB, HB, CHL, & Warm Sections	JLAB	Herb Strong
5			Ring and Transport Systems	BNL	PK Feng
	1		RF	BNL	Alex Zaltman
	2		Extraction Kicker	BNL	PK Feng
	3		Magnet HEBT	BNL	Ioannis Marnaris
	4		Magnet RTBT	BNL	Jian Lin Mi
	5		Magnet Ring	BNL	PK Feng
	6		Diagnostics	BNL	Pete Cameron
	7		Vacuum	BNL	Lorlei Smart, John Smith
	8		Miscellaneous	BNL	PK Feng
	9		Controls	BNL	John Smith
6			Target Systems	ORNL	Ron Battle
			Controls	ORNL	Ron Battle
			Cold Source	ORNL	Allen Crabtree
			Remote Control	ORNL	Mark Renich
7			Experiment Systems	SNS	Rick Riedel
8			Conventional Facilities Systems	SNS	Les Ottinger
	1-8		Power, Fire Alarm, Security, Office Network, etc.	SNS	Les Ottinger
	9		CF Controls	SvT	Randall Steadmon
9			Integrated Control Systems		Bill DeVan

(1) 3rd digit exists for all accelerator areas, but is only shown where needed to assign blocks of numbers.

SNS RF Control System

Table 14-3. RFCS Cable Numbering Scheme

1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	
Area Code from Table 14-1			Klystron Number		User-Defined		Description
3	2	B					Front End RF Controls – RFQ
4	2	C					Linac RF Controls – LEBT
4	2	D					Linac RF Controls – MEBT
4	2	E					Linac RF Controls – DTL
4	2	F					Linac RF Controls – CCL
4	2	G					Linac RF Controls – MB SRF
4	2	H					Linac RF Controls – HB SRF
4	2	L					Linac RF Controls – HEBT
			0	0			No specific Klystron – Applies to all
			0-9	1-9			Klystron Numbers 01 → 99
			A	0-9			Klystron Numbers 100 → 109
			B - Z	A - Z			Reserved for future use
					0	1 - Z	Cavity field probes (RF)
					1	1 - Z	Cavity forward power (RF)
					2	1 - Z	Cavity reflected power (RF)
					3	1 - Z	Cavity field probes (IF)
					4	1 - Z	HPRF & diagnostic interfaces (includes splitter & circulator load monitors)
					5	1 - Z	RFCS communications interfaces (MPS, RF_PERMIT, etc.)
					6	1 - Z	RFCS Internal Interfaces (intra-rack & intra-crate)
					7	1 - Z	Reference line, local oscillators, & associated interfaces
					8	1 - Z	RFCS fiber optic data links
					9	1 - Z	Signals/cables not otherwise classified (includes instrumentation probes)
					A - Z	1 - Z	Reserved for future use

Notes:

1. Klystrons are numbered sequentially beginning at 01 at the RFQ. Klystron numbers greater than 99 begin with “A”. e.g.: Klystron number 103 is number A3. Klystron numbers beginning with “B” and above are reserved for future use.
2. Cables are numbered sequentially in the sequence 1-9 followed by A, B, C, D, E, F, G, H, J, K, L, M, N, P, R, S, T, U, W, X, Y, Z. Note that I, O, Q, and V are omitted to avoid confusion with similar letters/numbers. This scheme permits 32 cables to be assigned to each function defined by the sixth digit in the cable number.

Example:

Cable number 42E.0531 is the first cavity reflected power cable for klystron 05 (from 0531). It is located in the DTL (from 42E).

15 Appendix Three – RFCS Cable Lists

Table 15-1. RFCS RFQ Cables

Cable Number	RFCS Signal	Subsystem	RFQ Signal Description (Signal – Media -- Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	CAV_FLD_IF	RACK	50 MHz IF / +20 dBm – 0.375 Heliac from REF mixer in tunnel to rack top -- Cavity phase/amplitude reference for FRCM.	NM → NM	1		
	CAV_FLD_IF	FRCM	50 MHz IF / +10 dBm – LMR-195 from rack top to FRCM CAV_FLD -- Cavity phase/amplitude reference for FRCM.	NF → PKZ			1
	CAV_FLD_RF	RACK	402.5 MHz / +20 dBm -- 0.375 Heliac from cavity pickup loop in tunnel to rack top -- Cavity field reference for HPM arc detect.	NM → NM	1		
	CAV_FLD_RF	HPM	402.5 MHz / +10 dBm – LMR-195 from rack top to HPM -- Cavity field reference for HPM arc detect.	NF → PKZ			1
	CAV_FLD_RF_MIX	REF	402.5 MHz / +20 dBm -- 0.375 Heliac from dedicated cavity pickup loop to REF mixer RF port (in tunnel) – This is a different pickup loop than that used for CAV_FLD_RF and HPM arc detect.	NM → NM	1		
	CAV_FWD_RF	RACK	402.5 MHz / +20 dBm -- 0.375 Heliac from klystron gallery directional coupler to rack top coaxial 2-way splitter – Forward power between circulator and 8-way WG splitter.	NM → NM		1	
	CAV_FWD_RF	HPM	402.5 MHz / +10 dBm – LMR-195 from rack top coaxial 2-way splitter to HPM – Forward power between circulator and 8-way WG splitter.	NF → PKZ			1
	CAV_FWD_RF	FRCM	402.5 MHz / +10 dBm – LMR-195 from rack top coaxial 2-way splitter to FRCM – Forward power between circulator and 8-way WG splitter.	NF → PKZ			1
	CAV_PU_[15..8]	RACK	402.5 MHz / +20 dBm -- 0.375 Heliac from tunnel to rack top -- Cavity field probes for instrumentation mux. (8 each)	NM → NM	8		
	CAV_PU_[15..8]	MUX_2	402.5 MHz / +10 dBm - LMR-195 from rack top to MUX_2 inputs (8 each) Instrumentation channels.	NF → SMA-M			8
	CAV_PU_[7..0]	RACK	402.5 MHz / +20 dBm 0.375 Heliac from 1 to rack top – Cavity field probes for instrumentation mux. (8 each)	NM → NM	8		
	CAV_PU_[7..0]	MUX_1	402.5 MHz / +10 dBm – LMR-195 from rack top to MUX_1 inputs (8 each) – Instrumentation channels.	NF → SMA-M			8
	CAV_RFL_RF_1	RACK	402.5 MHz / +20 dBm -- 0.375 Heliac from klystron gallery directional coupler to rack-top coaxial 2-way splitter – Reflected power between circulator and 8-way WG splitter.	NM → NM		1	

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Cable Number	RFCS Signal	Subsystem	RFQ Signal Description (Signal – Media -- Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	CAV_RFL_RF_1	HPM	402.5 MHz / +10 dBm – LMR-195 from rack top coaxial 2-way splitter to HPM – Reflected power between circulator and 8-way WG splitter.	NF → PKZ			1
	CAV_RFL_RF_1	FRCM	402.5 MHz / +10 dBm – LMR-195 from rack top coaxial 2-way splitter to FRCM – Reflected power between circulator and 8-way WG splitter.	NF → PKZ			1
	CIR_LD_RF	RACK	402.5 MHz / +20 dBm -- 0.375 Heliac from circulator load directional coupler reflected port to rack top. Used to detect failed circulator load.	NM → NM		1	
	CIR_LD_RF	HPM	402.5 MHz / +10 dBm – LMR-195 from rack top to HPM.	NF → PKZ			1
	CNTL_1 CNTL_2	REF	24VDC -- Switched +24VDC to heater control relays in the tunnel – four wire shielded twisted pair.	Term strip?	1		
	EVENT_LINK	UTIL	TSP from EVENT_LINK distribution to Utility Module	TBD			1
	EVENT_LINK	TIME	TSP from EVENT_LINK distribution to Timing Module	TBD			1
	FO_IQ	FRCM	Digital FO – Duplex Fiber optic cable (cable/connectors TBD) output from RFCS rack to control room with I/Q serial data.	FO TBD			1
	FOARC_[13..0]	HPM	TTL-Opto Isolator drive – 25 conductor shielded control cable to HPM FOARC -- FOARC signal from HPRF rack. HIGH = OK. The HPM connector is an AMP 748481-5 right angle female 25 pin high density D-Sub connector.	TBD – 25 pin female HD D-Sub		1	
	IF_50	CDM	Thin coax from CDM to FRCM	Lemo → Lemo			1
	LO_352	RACK	352.5 MHz/ +20 dBm LO - 0.375 Heliac from tunnel reference line coupler to rack top – CDM LO input	NM → NM	1		
	LO_352	FRCM	352.5 MHz / +10 dBm LO -- LMR-195 LO signal from CDM LO_OUT to FRCM LO_IN – LO for FRCM	PKZ → PKZ			1
	LO_352	CDM	352.5 MHz / +10 dBm LO -- LMR-195 LO signal from rack top to CDM LO_IN – LO reference for local RFCS	NF → PKZ			1
	MUX_1	HPM	402.5 MHz/+10 dBm – LMR-195 from MUX_1 output to HPM.	SMA-M → PKZ			1
	MUX_2	HPM	402.5 MHz/+10 dBm – LMR-195 from MUX_1 output to HPM.	SMA-M → PKZ			1
	PREPULSE	CDM	TTL PREPULSE signal from Timing Module to CDM	Lemo 50 Ohm			1
	PRT_1 PRT_2	REF	DC / Low current -- Inputs from Platinum Resistance Thermometers (PRT) in the reference line to reference line temperature controller in RFCS rack -- 8 shielded twisted pairs, 4 wire Kelvin connection for each.	Term Strip?	1		

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Cable Number	RFCS Signal	Subsystem	RFQ Signal Description (Signal – Media -- Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	REF_2.5_IN	RACK	2.500 MHz / TBD dBm Sync - 0.375 Heliac from master oscillator rack to REF_2.5 directional coupler in the RFCS rack.	NM → NM		1	
	REF_2.5_IN	CDM	2.500 MHz / TBD dBm Sync - LMR-195 from REF_2.5 directional coupler in RFCS rack to CDM	NF → PKZ			1
	REF_2.5_OUT	RACK	2.500 MHz / TBD dBm Sync - 0.375 Heliac from RFCS rack top to diagnostics rack. Provides diagnostics with 2.500 MHz reference.	NM → NM		1	
	REF_2.5_OUT	CDM	2.500 MHz / TBD dBm Sync - LMR-195 from CDM REF_OUT to RFCS rack top.	NF → PKZ			1
	RF_GATE	CDM	Thin coax from Timing Module to CDM	TBD → Lemo			1
	RF_OUT	RACK	402.5 MHz / +12 dBm max – 0.375 Heliac from RFCS rack to transmitter – Transmitter feed from FRCM	NM → NM		1	
	RF_OUT	FRCM	402.5 MHz / +12 dBm max -- LMR-195 from FRCM to rack top -- Transmitter feed from FRCM	PKZ → NF			1
	RF_PERMIT RF_FAULT*	MPS	Opto-Isolated TTL – Shielded twisted pair from TBD system to HPM. Opto-Isolated TTL -- Shielded twisted pair from HPM to MPS HPM end is 9 pin Micro D-sub Female.	TBD & TBD → Micro D- sub			1
	RFQ_FWD_[7..0]	RACK	402.5 MHz / +20 dBm -- 0.375 Heliac from tunnel to rack top – Forward power into RFQ for instrumentation mux. (8 each)	NM → NM	8		
	RFQ_FWD_[7..0]	MUX_2	402.5 MHz / +10 dBm – LMR-195 from rack top to MUX_1 inputs (8 each) – Instrumentation channels.	NF → SMA-M			8
	RFQ_RFL_[7..0]	RACK	402.5 MHz / +20 dBm 0.375 Heliac from tunnel to rack top -- Reflected power from RFQ for instrumentation mux. (8 each)	NM → NM	8		
	RFQ_RFL_[7..0]	MUX_1	402.5 MHz / +10 dBm – LMR-195 from rack top to MUX_2 inputs (8 each)	NF → SMA-M			8
	RS-232 COM	REF	RS-232 – Shielded twisted pair cable and connector TBD -- Bi-directional RS-232 communications between REF heater controller and EPICS IOC.	TBD		1	
	RTDL	UTIL	TSP from RTDL to Utility Module	TBD			1
	SAMPLE	CDM	Thin coax from Timing Module to CDM	TBD → Lemo			1

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Table 15-2. RFCS DTL Cables

Number	RFCS Signal	Subsystem	DTL Signal Description (Signal – Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	BEAM_FF	RACK	402.5 MHz / +20 dBm -- 0.375 Heliac from diagnostics rack to RFCS rack top -- Beam feed forward input from Diagnostic Group Rack	TBD → NM		1	
	BEAM_FF	FRCM	402.5 MHz / +20 dBm – LMR-195 rack top to FRCM -- Beam feed forward input from rack top to FRCM	NF → PKZ			1
	CAV_FLD_IF	RACK	50 MHz IF / +20 dBm – 0.375 Heliac from REF mixer in tunnel to rack top - Cavity phase/amplitude reference for FRCM	NM → NM	1		
	CAV_FLD_IF	FRCM	50 MHz IF / +10 dBm – LMR-195 from rack top to FRCM - Cavity phase/amplitude reference for FRCM	NF → PKZ			1
	CAV_FLD_RF	RACK	402.5 MHz / +20 dBm - 0.375 Heliac from cavity pickup loop in tunnel to rack top - Cavity field reference for HPM arc detect.	NM → NM	1		
	CAV_FLD_RF	HPM	402.5 MHz / +10 dBm – LMR-195 from rack top to HPM - Cavity field reference for HPM arc detect.	NF → PKZ			1
	CAV_FLD_RF_MIX	REF	402.5 MHz / +21 dBm - 0.375 Heliac from dedicated cavity pickup loop to REF mixer RF port (in tunnel). This is a different pickup loop than that used for CAV_FLD_RF and HPM arc detect.	NM → NM	1		
	CAV_FWD_RF	RACK	402.5 MHz / +20 dBm - 0.375 Heliac from WG directional coupler to splitter at rack top - Forward power between circulator and cavity.	NM → NM		1	
	CAV_FWD_RF	HPM	402.5 MHz / +10 dBm – LMR-195 from rack top splitter to HPM - Forward power between circulator and cavity.	NF → PKZ			1
	CAV_FWD_RF	FRCM	402.5 MHz / +10 dBm – LMR-195 from rack top splitter to FRCM - Forward power between circulator and cavity.	NF → PKZ			1
	CAV_PHS_DN	Tunnel	402.5 MHz / +7 dBm max – 0.375 Heliac - Cavity phase reference from downstream cavity to phase detector point in gallery. In thermal equilibrium with CAV_PHS_UP. Terminated when not in use.	NM → NM	1		
	CAV_PHS_UP	Tunnel	402.5 MHz / +7 dBm max – 0.375 Heliac - Cavity phase reference from upstream cavity to phase detector point in gallery. In thermal equilibrium with CAV_PHS_DN. Terminated when not in use.	NM → NM	1		
	CAV_PU	RACK	402.5 MHz / +20 dBm - 0.375 Heliac from cavity pickup loop in tunnel to rack top – Instrumentation cavity field probe.	NM → NM	1		
	CAV_PU	HPM	402.5 MHz / +10 dBm – LMR-195 from rack top to HPM - Instrumentation cavity field probe.	NF → PKZ			1
	CAV_RFL_RF_1	RACK	402.5 MHz / +20 dBm - 0.375 Heliac from klystron gallery directional coupler to rack-top 2-7way splitter – Reflected power between circulator and cavity.	NM → NM		1	

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Number	RFCS Signal	Subsystem	DTL Signal Description (Signal - Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	CAV_RFL_RF_1	HPM	402.5 MHz / +10 dBm – LMR-195 from 2-way splitter at top of rack to HPM – Reflected power between circulator and cavity.	NM → PKZ			1
	CAV_RFL_RF_1	FRCM	402.5 MHz / +10 dBm – LMR-195 from 2-way splitter at top of rack to FRCM – Reflected power between circulator and cavity.	NM → PKZ			1
	CIR_LD_RF	RACK	402.5 MHz / +20 dBm - 0.375 Heliac from circulator load in klystron gallery to rack top. Reflected power from circulator load to detect load failure.	NM → NM		1	
	CIR_LD_RF	HPM	402.5 MHz / +10 dBm – LMR-195 from rack top to HPM – Reflected power from circulator load to detect load failure.	NF → PKZ			1
	CNTL_1 CNTL_2	REF	24VDC - Switched +24VDC to heater control relays in the tunnel – four wire shielded twisted pair.	Term strip?	1		
	EVENT_LINK	UTIL	TSP from EVENT_LINK distribution to Utility Module	TBD			1
	EVENT_LINK	TIME	TSP from EVENT_LINK distribution to Timing Module	TBD			1
	FO_IQ	FRCM	Digital FO – Duplex Fiber optic cable (cable/connectors TBD) output from RFCS rack to control room with I/O serial data.	TBD			1
	FOARC_[7..0]	HPM	TTL-Opto Isolator drive – 25 conductor shielded control cable to HPM FOARC -- FOARC signal from HPRF rack. HIGH = OK. The HPM connector is an AMP 748481-5 right angle female 25 pin high density D-Sub connector.	TBD – 25 pin female HD D-Sub		1	
	IF_50	CDM	Thin coax from CDM to FRCM	Lemo → Lemo			1
	LO_352	RACK	352.5 MHz / +20 dBm LO – 0.375 Heliac from tunnel reference line coupler to rack top – LO for local RFCS	NM → NM	1		
	LO_352	FRCM	352.5 MHz / +10 dBm LO - LMR-195 LO signal from CDM LO_OUT to FRCM LO_IN – LO for FRCM	PKZ → PKZ			1
	LO_352	CDM	352.5 MHz / +10 dBm LO - LMR-195 LO signal from rack top to CDM LO_IN – LO for CDM	NF → PKZ			1
	PREPULSE	CDM	TTL PREPULSE signal from Timing Module to CDM	Lemo 50 Ohm			1
	PRT_1 PRT_2	REF	DC / Low current - Inputs from Platinum Resistance Thermometers (PRT) in the reference line to reference line temperature controller in RFCS rack - 8 shielded twisted pairs, 4 wire Kelvin connection for each.	Term Strip?			1
	REF_2.5_IN	RACK	2.500 MHz / TBD dBm Sync - 0.375 Heliac from master oscillator rack to REF_2.5 directional coupler in the RFCS rack.	NM → NM		1	
	REF_2.5_IN	CDM	2.500 MHz / TBD dBm Sync - LMR-195 from REF_2.5 directional coupler in RFCS rack to CDM	NF → PKZ			1
	REF_2.5_OUT	RACK	2.500 MHz / TBD dBm Sync - 0.375 Heliac from RFCS rack top to diagnostics rack. Provides diagnostics with 2.500 MHz reference.	NM → NM		1	
	REF_2.5_OUT	CDM	2.500 MHz / TBD dBm Sync - LMR-195 from CDM REF_OUT to RFCS rack top.	NF → PKZ			1
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Number	RFCS Signal	Subsystem	DTL Signal Description (Signal – Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	RF_GATE	CDM	Thin coax from Timing Module to CDM	TBD → Lemo			1
	RF_OUT	RACK	402.5 MHz / +12 dBm max – 0.375 Heliax from RFCS rack to transmitter – transmitter feed from FRCM	NM → NM		1	
	RF_OUT	FRCM	402.5 MHz / +12 dBm max - LMR-195 from FRCM to rack top -- transmitter feed from FRCM	PKZ → NF			1
	RF_PERMIT RF_FAULT*	MPS	Opto-Isolated TTL – Shielded twisted pair from TBD system to HPM Opto-Isolated TTL -- Shielded twisted pair from HPM to MPS HPM end is 9 pin Micro D-sub Female.	TBD & TBD → Micro D-sub			1
	RS-232 COM	REF	RS-232 – Shielded twisted pair cable and connector TBD -- Bi-directional RS-232 communications between REF heater controller and EPICS IOC.	TBD		1	
	RTDL	UTIL	TSP from RTDL to Utility Module	TBD			1
	SAMPLE	CDM	Thin coax from Timing Module to CDM	TBD → Lemo			1

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Table 15-3. RFCS CCL Cables

Number	RFCS Signal	Subsystem	CCL Signal Description (Signal – Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	BEAM_FF	RACK	805 MHz / +20 dBm -- 0.375 Helix from diagnostics rack to RFCS rack top -- Beam feed forward input from Diagnostic Group Rack.	TBD → NM		1	
	BEAM_FF	FRCM	805 MHz / +20 dBm – LMR-195 rack top to FRCM - - Beam feed forward input from rack top to FRCM.	NF → PKZ			1
	CAV_FLD_IF	RACK	50 MHz IF / +20 dBm – 0.375 Helix from REF mixer in tunnel to rack top - Cavity phase/amplitude reference for FRCM.	NM → NM	1		
	CAV_FLD_IF	FRCM	50 MHz IF / +10 dBm – LMR-195 from rack top to FRCM - Cavity phase/amplitude reference for FRCM.	NF → PKZ			1
	CAV_FLD_RF	RACK	805 MHz / +20 dBm - 0.375 Helix from cavity pickup loop in tunnel to rack top - Cavity field reference for HPM arc detect.	NM → NM	1		
	CAV_FLD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM - Cavity field reference for HPM arc detect.	NM → PKZ			1
	CAV_FLD_RF_MIX	REF	805 MHz / +21 dBm - 0.375 Helix from dedicated cavity pickup loop to REF mixer RF port (in tunnel). This is a different pickup loop than that used for CAV_FLD_RF and HPM arc detect.	NM → NM	1		
	CAV_FWD_RF	RACK	805 MHz / +20 dBm - 0.375 Helix from WG directional coupler to rack top splitter - Forward power between circulator and WG splitter.	NM → NM		1	
	CAV_FWD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top splitter to HPM- Forward power between circulator and WG splitter.	NF → PKZ			1
	CAV_FWD_RF	FRCM	805 MHz / +10 dBm – LMR-195 from rack top to FRCM - Forward power between circulator and WG splitter.	NF → PKZ			1
	CAV_PHS_DN	Tunnel	805 MHz / +7 dBm max – LMR-195 - Cavity phase reference from downstream cavity to phase detector point in gallery. In thermal equilibrium with CAV_PHS_UP. Terminated when not in use.	SMA_M → SMA-M	1		
	CAV_PHS_UP	Tunnel	805 MHz / +7 dBm max – LMR-195 - Cavity phase reference from upstream cavity to phase detector point in gallery. In thermal equilibrium with CAV_PHS_DN. Terminated when not in use.	SMA_M → SMA-M	1		
	CAV_PU	RACK	805 MHz / +20 dBm - 0.375 Helix from cavity pickup loop in tunnel to rack top – Instrumentation cavity field probe.	NM → NM	1		
	CAV_PU	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM - Instrumentation cavity field probe.	NF → PKZ			1
	CAV_RFL_RF_1	RACK	805 MHz / +20 dBm – 0.375 Helix from tunnel WG directional coupler to rack-top 2-way splitter – Reflected power between splitter and cavity port 1.	NM → NM	1		

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Number	RFCS Signal	Subsystem	CCL Signal Description (Signal - Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	CAV_RFL_RF_1	HPM	805 MHz / +10 dBm – LMR-195 from 2-way splitter at top of rack to HPM – Reflected power between WG splitter and cavity port 1	NF → PKZ			1
	CAV_RFL_RF_1	FRCM	805 MHz / +10 dBm – LMR-195 from 2-way splitter at top of rack to FRCM – Reflected power between WG splitter and cavity port 1.	NF → PKZ			1
	CAV_RFL_RF_2	RACK	805 MHz / +20 dBm – 0.375 Heliac from tunnel WG directional coupler to rack-top – Reflected power between splitter and cavity port 2	NM → NM	1		
	CAV_RFL_RF_2	HPM	805 MHz / +10 dBm – LMR-195 from top of rack to HPM – Reflected power between WG splitter and cavity port 2	NF → PKZ			1
	CIR_LD_RF	RACK	805 MHz / +20 dBm - 0.375 Heliac from circulator load in klystron gallery to rack top. Reflected power from circulator load to detect load failure.	NM → NM		1	
	CIR_LD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM – Reflected power from circulator load to detect load failure..	NF → PKZ			1
	CNTL_1 CNTL_2	REF	24VDC - Switched +24VDC to heater control relays in the tunnel – four wire shielded twisted pair.	Term strip?	1		
	EVENT_LINK	UTIL	TSP from EVENT_LINK distribution to Utility Module	TBD			1
	EVENT_LINK	TIME	TSP from EVENT_LINK distribution to Timing Module	TBD			1
	FO_IQ	FRCM	Digital FO – Duplex Fiber optic cable (cable/connectors TBD) output from RFCS rack to control room with I/Q serial data.	FO TBD			1
	FOARC_[10..0]	HPM	TTL-Opto Isolator drive – 25 conductor shielded control cable to HPM FOARC -- FOARC signal from HPRF rack. HIGH = OK. The HPM connector is an AMP 748481-5 right angle female 25 pin high density D-Sub connector.	TBD – 25 pin female HD D-Sub		1	
	IF_50	CDM	Thin coax from CDM to FRCM	Lemo → Lemo			1
	LO_755	RACK	755 MHz/ +20 dBm LO - 0.375 Heliac from tunnel reference line coupler to rack top – LO for RFCS	NM → NM	1		
	LO_755	FRCM	755 MHz / +10 dBm LO - LMR-195 LO signal from CDM LO_OUT to FRCM LO_IN.	PKZ → PKZ			1
	LO_755	CDM	755 MHz / +10 dBm LO - LMR-195 LO signal from rack top to CDM LO_IN	NF → PKZ			1
	PREPULSE	CDM	TTL PREPULSE signal from Timing Module to CDM	Lemo 50 Ohm			1
	PRT_1 PRT_2	REF	DC / Low current - Inputs from Platinum Resistance Thermometers (PRT) in the reference line to reference line temperature controller in RFCS rack - 8 shielded twisted pairs, 4 wire Kelvin connection for each.	Term Strip?	1		
	REF_2.5_IN	RACK	2.500 MHz / TBD dBm Sync - 0.375 Heliac from master oscillator rack to REF_2.5 directional coupler in the RFCS rack.	NM → NM		1	

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Number	RFCS Signal	Subsystem	CCL Signal Description (Signal - Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	REF_2.5_IN	CDM	2.500 MHz / TBD dBm Sync - LMR-195 from REF_2.5 directional coupler in RFCS rack to CDM	NF → PKZ			1
	REF_2.5_OUT	RACK	2.500 MHz / TBD dBm Sync - 0.375 Heliac from RFCS rack top to diagnostics rack. Provides diagnostics with 2.500 MHz reference.	NM → NM		1	
	REF_2.5_OUT	CDM	2.500 MHz / TBD dBm Sync - LMR-195 from CDM REF_OUT to RFCS rack top.	NF → PKZ			1
	RF_GATE	CDM	Thin coax from Timing Module to CDM	TBD → Lemo			1
	RF_OUT	RACK	805 MHz / +12 dBm max – 0.375 Heliac from RFCS rack to transmitter – Transmitter feed from FRCM	NM → NM		1	
	RF_OUT	FRCM	805 MHz / +12 dBm max - LMR-195 from FRCM to rack top - Transmitter feed from FRCM	PKZ → NF			1
	RF_PERMIT RF_FAULT*	MPS	Opto-Isolated TTL – Shielded twisted pair from TBD system to HPM Opto-Isolated TTL -- Shielded twisted pair from HPM to MPS HPM end is 9 pin Micro D-sub Female.	TBD & TBD → Micro D-sub			1
	RS-232 COM	REF	RS-232 – Shielded twisted pair cable and connector TBD -- Bi-directional RS-232 communications between REF heater controller and EPICS IOC.	TBD		1	
	RTDL	UTIL	TSP from RTDL to Utility Module	TBD			1
	SAMPLE	CDM	Thin coax from Timing Module to CDM	TBD → Lemo			1
	SPLIT_LD_RF	RACK	805 MHz / +20 dBm - 0.375 Heliac from splitter load in klystron gallery to rack top. Reflected power from splitter load to detect load failure.	NM → NM		1	
	SPLIT_LD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM – Reflected power from splitter load to detect load failure.	NF → PKZ			1

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Table 15-4. RFCS SRF Cables

Number	RFCS Signal	Subsystem	SRF Signal Description (Signal - Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	BEAM_FF	RACK	805 MHz / +20 dBm -- 0.375 Helix from diagnostics rack to RFCS rack top -- Beam feed forward input from Diagnostic Group Rack	TBD → NM		1	
	BEAM_FF	FRCM	805 MHz / +20 dBm – LMR-195 rack top to FRCM -- Beam feed forward input from rack top to FRCM BEAM_FF	NF → PKZ			1
	CAV_FLD_IF	RACK	50 MHz IF / +20 dBm – 0.375 Helix from REF mixer in tunnel to rack top - Cavity phase/amplitude reference for FRCM	NM → NM	1		
	CAV_FLD_IF	FRCM	50 MHz IF / +10 dBm – LMR-195 from rack top to FRCM - Cavity phase/amplitude reference for FRCM	NF → PKZ			1
	CAV_FLD_RF	RACK	805 MHz / +21 dBm - 0.375 Helix from cavity pickup loop to 2-way coaxial splitter in tunnel – Splitter Output 1: CAV_FLD_RF – Cavity field ref to HPM Splitter Output 2: CAV_FLD_RF_MIX – RF input to REF mixer RF port for downconversion to 50 MHz IF	NM → NM	1		
	CAV_FLD_RF	RACK	805 MHz / +14 dBm - 0.375 Helix from splitter in tunnel to rack top splitter - Cavity field reference for HPM arc detect.	NM → NM	1		
	CAV_FLD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM - Cavity field reference for HPM arc detect.	NF → PKZ			1
	CAV_FLD_RF_MIX	REF	805 MHz / +14 dBm - 0.375 Helix from splitter in tunnel to REF mixer RF port (in tunnel).	NM → NM	1		
	CAV_FWD_RF	RACK	805 MHz / +20 dBm - 0.375 Helix from WG directional coupler to rack top splitter - Forward power between circulator and cavity.	NM → NM		1	
	CAV_FWD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top splitter to HPM - Forward power between circulator and cavity.	NF → PKZ			1
	CAV_FWD_RF	FRCM	805 MHz / +10 dBm – LMR-195 from rack top splitter to FRCM - Forward power between circulator and cavity.	NF → PKZ			1
	CAV_RFL_RF_1	RACK	805 MHz / +20 dBm - 0.375 Helix from klystron gallery directional coupler to rack-top 2-way splitter – Reflected power between circulator and cavity.	NM → NM		1	
	CAV_RFL_RF_1	HPM	805 MHz / +10 dBm – LMR-195 from 2-way splitter at top of rack to HPM – Reflected power between circulator and cavity.	NF → PKZ			1
	CAV_RFL_RF_1	FRCM	805 MHz / +10 dBm – LMR-195 from 2-way splitter at top of rack to FRCM – Reflected power between circulator and cavity.	NF → PKZ			1
	CIR_LD_RF	RACK	805 MHz / +20 dBm - 0.375 Helix from circulator load in klystron gallery to rack top. Reflected power from circulator load to detect load failure.	NM → NM		1	

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Number	RFCS Signal	Subsystem	SRF Signal Description (Signal - Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	CIR_LD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top to FRM – Reflected power from circulator load to detect load failure.	NF → PKZ			1
	CNTL_1 CNTL_2	REF	24VDC - Switched +24VDC to heater control relays in the tunnel – four wire shielded twisted pair.	Term strip?	1		
	EVENT_LINK	UTIL	TSP from EVENT_LINK distribution to Utility Module	TBD			1
	EVENT_LINK	TIME	TSP from EVENT_LINK distribution to Timing Module	TBD			1
	FO_IQ	FRCM	Digital FO – Duplex Fiber optic cable (cable/connectors TBD) output from RFCS rack to control room with I/Q serial data.	FO TBD			1
	FOARC_[4..0]	HPM	TTL-Opto Isolator drive – 25 conductor shielded control cable to HPM FOARC -- FOARC signal from HPRF rack. HIGH = OK. The HPM connector is an AMP 748481-5 right angle female 25 pin high density D-Sub connector.	TBD – 25 pin female HD D-Sub		1	
	IF_50	CDM	Thin coax from CDM to FRCM	Lemo → Lemo			1
	KLY_FWD_RF	RACK	805 MHz / +20 dBm - 0.375 Heliac from HPRF transmitter rack splitter in klystron gallery to RFCS rack top. Forward power out of klystron.	NM → NM		1	
	KLY_FWD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM – Forward power out of klystron.	NF → PKZ			1
	KLY_RFL_RF	RACK	805 MHz / +20 dBm - 0.375 Heliac from HPRF transmitter rack splitter in klystron gallery to RFCS rack top. Reflected power between klystron and circulator.	NM → NM		1	
	KLY_RFL_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM – Reflected power between klystron and circulator.	NF → PKZ			1
	LO_755	RACK	755 MHz / +20 dBm LO - 0.375 Heliac from tunnel reference line coupler to rack top	NM → NM	1		
	LO_755	FRCM	755 MHz / +10 dBm LO - LMR-195 LO signal from CDM to FRCM	PKZ → PKZ			1
	LO_755	CDM	755 MHz / +10 dBm LO - LMR-195 LO signal from rack top to CDM	NF → PKZ			1
	PREPULSE	CDM	TTL PREPULSE signal from Timing Module to CDM	Lemo 50 Ohm			1
	PRT_1 PRT_2	REF	DC / Low current - Inputs from Platinum Resistance Thermometers (PRT) in the reference line to reference line temperature controller in RFCS rack - 8 shielded twisted pairs, 4 wire Kelvin connection for each.	TERM STRIP?	1		
	REF_2.5_IN	RACK	2.500 MHz / TBD dBm Sync - 0.375 Heliac from master oscillator rack to REF_2.5 directional coupler in the RFCS rack.	NM → NM		1	
	REF_2.5_IN	CDM	2.500 MHz / TBD dBm Sync - LMR-195 from REF_2.5 directional coupler in RFCS rack to CDM	NF → PKZ			1
	REF_2.5_OUT	RACK	2.500 MHz / TBD dBm Sync - 0.375 Heliac from RFCS rack top to diagnostics rack. Provides diagnostics with 2.500 MHz reference.	NM → NM		1	

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Number	RFCS Signal	Subsystem	SRF Signal Description (Signal - Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	REF_2.5_OUT	CDM	2.500 MHz / TBD dBm Sync - LMR-195 from CDM REF_OUT to RFCS rack top.	NF → PKZ			1
	RF_GATE	CDM	Thin coax from Timing Module to CDM	TBD → Lemo			1
	RF_OUT	RACK	805 MHz / +12 dBm max - 0.375 Heliac from RFCS rack to transmitter - Transmitter feed from FRCM	NM → NM		1	
	RF_OUT	FRCM	805 MHz / +12 dBm max - LMR-195 from FRCM to rack top - Transmitter feed from FRCM	PKZ → NF			1
	RF_PERMIT RF_FAULT*	MPS	Opto-Isolated TTL - Shielded twisted pair from TBD system to HPM Opto-Isolated TTL -- Shielded twisted pair from HPM to MPS HPM end is 9 pin Micro D-sub Female.	TBD & TBD → Micro D-sub			1
	RS-232 COM	REF	RS-232 - Shielded twisted pair cable and connector TBD -- Bi-directional RS-232 communications between REF heater controller and EPICS IOC.	TBD		1	
	RTDL	UTIL	TSP from RTDL to Utility Module	TBD			1
	SAMPLE	CDM	Thin coax from Timing Module to CDM	TBD → Lemo			1

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Table 15-5. RFCS HEBT Cables

Number	RFCS Signal	Subsystem	HEBT Signal Description (Signal – Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	BEAM_FF	RACK	805 MHz / +20 dBm -- 0.375 Heliac from diagnostics rack to RFCS rack top -- Beam feed forward input from Diagnostic Group Rack.	TBD → NM		1	
	BEAM_FF	FRCM	805 MHz / +20 dBm – LMR-195 rack top to FRCM - Beam feed forward input rack top to FRCM.	NF → PKZ			1
	CAV_FLD_IF	RACK	50 MHz IF / +20 dBm – 0.375 Heliac from REF mixer in tunnel to rack top - Cavity phase/amplitude reference for FRCM.	NM → NM	1		
	CAV_FLD_IF	FRCM	50 MHz IF / +10 dBm – LMR-195 from rack top to FRCM - Cavity phase/amplitude reference for FRCM.	NF → PKZ			1
	CAV_FLD_RF	RACK	805 MHz / +20 dBm - 0.375 Heliac from cavity pickup loop in tunnel to rack top - Cavity field reference for HPM arc detect.	NM → NM	1		
	CAV_FLD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM - Cavity field reference for HPM arc detect.	NF → PKZ			1
	CAV_FLD_RF_MIX	REF	805 MHz / +21 dBm - 0.375 Heliac from dedicated cavity pickup loop to REF mixer RF port (in tunnel). This is a different pickup loop than that used for CAV_FLD_RF and HPM arc detect.	NM → NM	1		
	CAV_FWD_RF	RACK	805 MHz / +20 dBm - 0.375 Heliac from WG directional coupler to splitter on rack top - Forward power between circulator and cavity.	NM → NM		1	
	CAV_FWD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM - Forward power between circulator and cavity.	NF → PKZ			1
	CAV_FWD_RF	FRCM	805 MHz / +10 dBm – LMR-195 from rack top splitter to FRCM - Forward power between circulator and cavity.	NF → PKZ			1
	CAV_PHS_DN	Tunnel	805 MHz / +7 dBm max – LMR-195 - Cavity phase reference from downstream cavity to phase detector point in gallery. In thermal equilibrium with CAV_PHS_UP. Terminated when not in use.	SMA_M → SMA-M	1		
	CAV_PHS_UP	Tunnel	805 MHz / +7 dBm max – LMR-195 - Cavity phase reference from upstream cavity to phase detector point in gallery. In thermal equilibrium with CAV_PHS_DN. Terminated when not in use.	SMA_M → SMA-M	1		
	CAV_PU	RACK	805 MHz / +20 dBm - 0.375 Heliac from cavity pickup loop in tunnel to rack top – Instrumentation cavity field probe.	NM → NM	1		
	CAV_PU	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM - Instrumentation cavity field probe.	NF → PKZ			1
	CAV_RFL_RF_1	RACK	805 MHz / +20 dBm - 0.375 Heliac from klystron gallery directional coupler to rack-top 2-way splitter – Reflected power between circulator and cavity.	NM → NM		1	

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Number	RFCS Signal	Subsystem	HEBT Signal Description (Signal – Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	CAV_RFL_RF_1	HPM	805 MHz / +10 dBm – LMR-195 from 2-way splitter at top of rack to HPM – Reflected power between circulator and cavity.	NF → PKZ			1
	CAV_RFL_RF_1	FRCM	805 MHz / +10 dBm – LMR-195 from 2-way splitter at top of rack to FRCM – Reflected power between circulator and cavity.	NF → PKZ			1
	CIR_LD_RF	RACK	805 MHz / +20 dBm - 0.375 Heliac from circulator load in klystron gallery to rack top. Reflected power from circulator load to detect load failure.	NM → NM		1	
	CIR_LD_RF	HPM	805 MHz / +10 dBm – LMR-195 from rack top to HPM - Reflected power from circulator load to detect load failure.	NF → PKZ			1
	CNTL_1 CNTL_2	REF	24VDC - Switched +24VDC to heater control relays in the tunnel – four wire shielded twisted pair.	Term strip?	1		
	EVENT_LINK	UTIL	TSP from EVENT_LINK distribution to Utility Module	TBD			1
	EVENT_LINK	TIME	TSP from EVENT_LINK distribution to Timing Module	TBD			1
	FO_IQ	FRCM	Digital FO – Duplex Fiber optic cable (cable/connectors TBD) output from RFCS rack to control room with I/Q serial data.	FO TBD			1
	FOARC_[7..0]	HPM	TTL-Opto Isolator drive – 25 conductor shielded control cable to HPM FOARC -- FOARC signal from HPRF rack. HIGH = OK. The HPM connector is an AMP 748481-5 right angle female 25 pin high density D-Sub connector.	TBD – 25 pin female HD D-Sub			1
	IF_50	CDM	Thin coax from CDM to FRCM	Lemo → Lemo			1
	LO_755	RACK	755 MHz/ +20 dBm LO - 0.375 Heliac from tunnel reference line coupler to rack top – LO reference for local RFCS	NM → NM	1		
	LO_755	FRCM	755 MHz / +10 dBm LO - LMR-195 LO signal from CDM LO_OUT to FRCM LO_IN	PKZ → PKZ			1
	LO_755	CDM	755 MHz / +10 dBm LO - LMR-195 LO signal from rack top to CDM LO_IN – Local LO reference.	NF → PKZ			1
	PREPULSE	CDM	TTL PREPULSE signal from Timing Module to CDM	Lemo 50 Ohm			1
	PRT_1 PRT_2	REF	DC / Low current - Inputs from Platinum Resistance Thermometers (PRT) in the reference line to reference line temperature controller in RFCS rack - 8 shielded twisted pairs, 4 wire Kelvin connection for each.	TERM STRIP?	1		
	REF_2.5_IN	RACK	2.500 MHz / TBD dBm Sync - 0.375 Heliac from master oscillator rack to REF_2.5 directional coupler in the RFCS rack.	NM → NM		1	
	REF_2.5_IN	CDM	2.500 MHz / TBD dBm Sync - LMR-195 from REF_2.5 directional coupler in RFCS rack to CDM	NF → PKZ			1
	REF_2.5_OUT	RACK	2.500 MHz / TBD dBm Sync - 0.375 Heliac from RFCS rack top to diagnostics rack. Provides diagnostics with 2.500 MHz reference.	NM → NM		1	

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Number	RFCS Signal	Subsystem	HEBT Signal Description (Signal – Media - Function)	Connector	In Tunnel	In Gallery	In RFCS Rack
	REF_2.5_OUT	CDM	2.500 MHz / TBD dBm Sync - LMR-195 from CDM REF_OUT to RFCS rack top.	NF → PKZ			1
	RF_GATE	CDM	Thin coax from Timing Module to CDM	TBD → Lemo			1
	RF_OUT	RACK	805 MHz / +12 dBm max – 0.375 Heliax from RFCS rack to transmitter – Transmitter feed from FRCM	NM → NM		1	
	RF_OUT	FRCM	805 MHz / +12 dBm max - LMR-195 from FRCM to rack top - Transmitter feed from FRCM	PKZ → NM			1
	RF_PERMIT RF_FAULT*	MPS	Opto-Isolated TTL – Shielded twisted pair from TBD system to HPM Opto-Isolated TTL -- Shielded twisted pair from HPM to MPS HPM end is 9 pin Micro D-sub Female.	TBD → Micro D-sub			1
	RS-232 COM	REF	RS-232 – Shielded twisted pair cable and connector TBD -- Bi-directional RS-232 communications between REF heater controller and EPICS IOC.	TBD		1	
	RTDL	UTIL	TSP from RTDL to Utility Module	TBD			1
	SAMPLE	CDM	Thin coax from Timing Module to CDM	TBD → Lemo			1

16 Appendix Four – Signal Technologies RF Multiplexer Interface

This document provided by Signal Technology and reformatted by Dave Thomson.

Signal Technology Systems Division

General Purpose VXI Board

Hardware Description And Test Document Rev 1.1

Date: Jun 6, 2001

Revisions:

Rev 1.0	Mar 28, 2001	RT	issue test document with hardware description included.
Rev 1.1	June 6 2001	RT	rename document . Add revision section Section 5 add chip select values to Register descriptions. RT 3-28-01

16.1 VXI general purpose IO board - Signal Technology P/ N PC-1056

The Signal technology PC1056 is a general purpose IO board for the VXI bus . It allows a user to mount a device to the board and provides general purpose IO lines for the user's application hardware and software.

This document describes the basic electronic features of the board and briefly how it interacts with the software, for the purpose of understanding how the board works so it may be tested/troubleshoot.

This card is a register based VXI module. It uses 16 bit addressing mode on the VXI bus. 24/32 bit modes are not supported. There are no interrupts used by the card.

16.2 Handling precautions.

- Be aware of static sensitive components.
- Be aware that the ferrite body of the inductors is fragile. L6 located near the edge of the board is somewhat vulnerable to handling damage.

16.3 Software

Two software programs are discussed in conjunction with this card.

SURM --is the HP Start-Up Resource Manager. At startup this program queries the card to determine and/or set it's configuration.

Signal Tech .exe – This Windows application is written to specifically work with this card to read and write the GP registers. It uses information in the card EEPROM. This software is described in a separate document.

16.4 Board Addressing

16.4.1 Card Address -- OFFSET write Register and Switch S1:

The Logical address (ULA) of the card is the base address offset which is stored on the card itself.

The OFFSET address is set at S1 OR if S1 is set to FF then the offset is written to the card at U2 when the MODID signal is sent from the master.

THE CARD IS SELECTED WHEN all of the following is true

- 1: Offset address matches S1 or the programmed value if S1 is set to 0xFF (U3)
- 2: A hex code of either 0x29 or 0x2D is present on AM0 - AM5. (U5)
- 3: A14 and A15 are both high . (U5)
- 4: LWORD is false .(U5)

16.4.2 VXI Automatic Module ID:

When the MODID signal is sent from the master and S1=0xFF then the PLD (U49), along with U9 and U10 provide the logic to clock the offset address from the master into U2. The output of U2 is tristate unless S1 is set to 0xFF.

Setting S1 to a value other than 0xFF over-rides the automatic Module ID function of VXI.

The application software requires a fixed ULA . This value is located in the SIGNAL TECH.INI file and is normally set for Port=15. This value should be set into the S1 switch .

Set 15 (0x0F) at S1 by setting switches 1-4 ON (High) and 5-8 OFF(Low).

The HP SURM program will accept the module at ULA15 .

Switch S1 is located at the upper edge of the board .

S1 8 7 6 5 4 3 2 1 correspond to bits 7 6 5 4 3 2 1 0

Move the switch up to set a "1" and down to set a "0"

16.5 BOARD REGISTERS

The address is latched at U7 and a one of 8 decoder (U1) further breaks down the address into 8 individual chip selects. The function of each of these chip selects is described next.

- **Chip select 0 Card ID**
- **Chip select 1 Device Type**

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- **Chip select 2** Status
- **Chip select 3** Offset
- **Chip select 4** GP Status /control A
- **Chip select 5** GP Status /control B
- **Chip select 6** GP Status /control C
- **Chip select 7** GP Status /control D

When the board is being accessed, the 16 bit board data bus DB[0..15] is enabled onto the system data bus D[0..15] at the data bus buffers (U11,13).

16.5.1 ID register – read only

The Card ID is a hardwired value representing certain information about the card:

DB14-15 set the VXIbus device classification – in this case 11 for **register based**.

DB12-13 set the Addressing Mode – in this case 11 for **A16 only**

DB 00-11 set the Manufacturer ID – in this case 0xE74 for **Signal Technology**

16.5.2 Device type Register --read only

The device type is a value that can be set for the card by the user. It is set at dip switches S2 and S3, and read back at the Device type register (U22, U24). S2 sets the high order bits and S3 sets the low order bits.

The switches are physically arranged on the board as shown below:

S3 1 2 3 4 5 6 7 8 = **Low order bits 7, 6, 5, 4, 3, 2, 1, 0**

S2 1 2 3 4 5 6 7 8 = **High order bits 15,14,13,12,11,10,9,8**

Move the switch down to set a “1” and up to set a “0” .

SURM reports the value of the device type register as the MODEL number. All 16 bits of the register are readable. However, by VXI convention the device type must be >255 so that the card will not be identified as a “slot 0 controller” by SURM.

16.5.3 Status Register – read cycle

The status register is required by VXI convention

This read register (U21,U23) allows the software to read the following signals:

MODID*	VXI backplane signal:
POWER_OK*, POWER_FAIL*	From the on-board window comparators
READY_ST, PASSED_ST	Signals from connector J5 – pulled HI on this card if open.

The serial EEPROM data is read at bit 8. The serial EEPROM contains values used by the software to interpret and scale the readings from the board general purpose IO.

The status register also contains several spare bits. A read of this register normally shows a value of 65471 decimal corresponding to all bits high except POWER_OK*

16.5.4 Status Register –write cycle

The status write register (U35,36) is where the EEPROM data out and write control bits are manipulated.. Note that the EEPROM program enable bit is pulled high to enable it. This can be wired low at PD109 to disable programming the EEPROM.

SWRESET_CTL* can be set here (routed to J5).

The other bits are spares.

16.5.5 OFFSET register –read only

The OFFSET value can be read back from the OFFSET register (U8). If this is set to 15 the value read back is 65295 or 1111 1111 0000 1111. The upper 8 bits are high and the lower 8 bits are set by S1 or the value written during MODID.

16.5.6 Board GP Status/control registers A,B,C,D (STAT/CTL) read-write

These are the general purpose registers that can be utilized to interface with user hardware. There are separate registers for read and write at each address. The signals from these registers are routed to connectors J6,J7,J8,and J9, for connection to 50 pin ribbon cables to the user's hardware.

Writing to any of these registers latches a value to the connector pin.

Reading the register reads a value from a connector pin.

16.6 LED Indicators

Voltage Supply and Monitor circuit:

The VXI bus provides +5V, +12V, -12V, +24V,-24V to the card. These are filtered and fused before being distributed to the on-board circuitry. A +5STDBY is generated from the +5V OR +12V. This powers comparators which monitor the voltage levels of the incoming power. The **GREEN LED** (POWER_OK*) is lit if ALL of the power supplies are within an expected tolerance, otherwise the **RED LED** (POWER_FAIL*) is lit. These signals are read by the status port.

The voltage range accepted for POWER_OK* -- GREEN status is approximately

+12V +10.8 to +13.2V

-12V -10.0 to -14.5V

+5V +4.87 to + 5.25V

+24V +20to +28V

-24V -20 to -28V

D5 provides the voltage reference. Window comparators for each supply are formed by U48,U52,U55.

16.6.1 Activity Monitor:

The **YELLOW LED** is lit whenever a read or write to the board is done. U47A stretches the pulse so the LED flash will be visible.

The Signal Technology application reads the board about once a second so the yellow LED will flash periodically.

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16.7 Loopback testing the general purpose registers

For testing the board a loopback plug can be made from a 50 pin ribbon receptacle so that data written to the control registers can be directly read back at a status register. A convenient way to do this simply connects together all the pins located directly across from each other, on each of the four connectors (J6,7,8,9) as follows:

Pin 7to8, 11 to12, 13 to14, etc. This makes for physically convenient wiring of the test plug but makes logically interpreting the data somewhat confusing since the bits are reversed left to right when read back , also the arrangement of each 16 bit word is swapped . This is discussed later in this document:

16.7.1 EEPROM setup:

Before doing loopback testing, the NVM –non-volatile memory values should be set as follows to do loopback testing:

Refer to the software spec for explanation of these values.

Upper_limit_0: >=4294967295 Lower_Limit_0 <= -4294967295 (allow full 64 bits to be used)

Scalar_0: 1 Offset_0: 0 (Scaling : gain=1 offset=0)
Digits_Left_0: 10 Digits_Right_0:0 (display digits xxxxxxxxxxx.)
BCD_0: not checked (see software spec)
Apply_Mode_0: not checked (see software spec)

Upper_limit_1: >=4294967295 Lower_Limit_1 <= -4294967295

Scalar_1: 1 Offset_1: 0
Digits_Left_1: 10 Digits_Right_1:0
BCD_1: not checked
Apply_Mode_1: not checked
Status Mask: FFFFFFFFFFFFFFFF (allow all bits to be displayed)

Once the NVM setup is established, values can be written to the control registers and read back at the status registers.

16.7.2 Examples of test pattern control values vs. expected status readback:

(Spaces added for clarity in this document. They are not shown in the actual display)

Entry_0 0x 0000 0000
Entry_1 0x 0000 0000
Status 0000 0000 0000 0000

Entry_0 0x 1111 1111 (because bit order is reversed 0001 reads back as 1000)

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Entry_1 0x 1111 1111
Status 8888 8888 8888 8888

Entry_0 0x 2222 2222 (because bit order is reversed 0010 reads back as 0100)
Entry_1 0x 2222 2222
Status 4444 4444 4444 4444

Entry_0 0x 0888 8888 (because bit order is reversed 1000 reads back as 0001)
Entry_1 0x 0888 8888
Status 1111 1110 1111 1110

(-3-26-01 current software version does not accept Msbit =1)

Entry_0 0x 5555 5555 (0101 reads back as 1010)
Entry_1 0x 5555 5555
Status aaaa aaaa aaaa aaaa

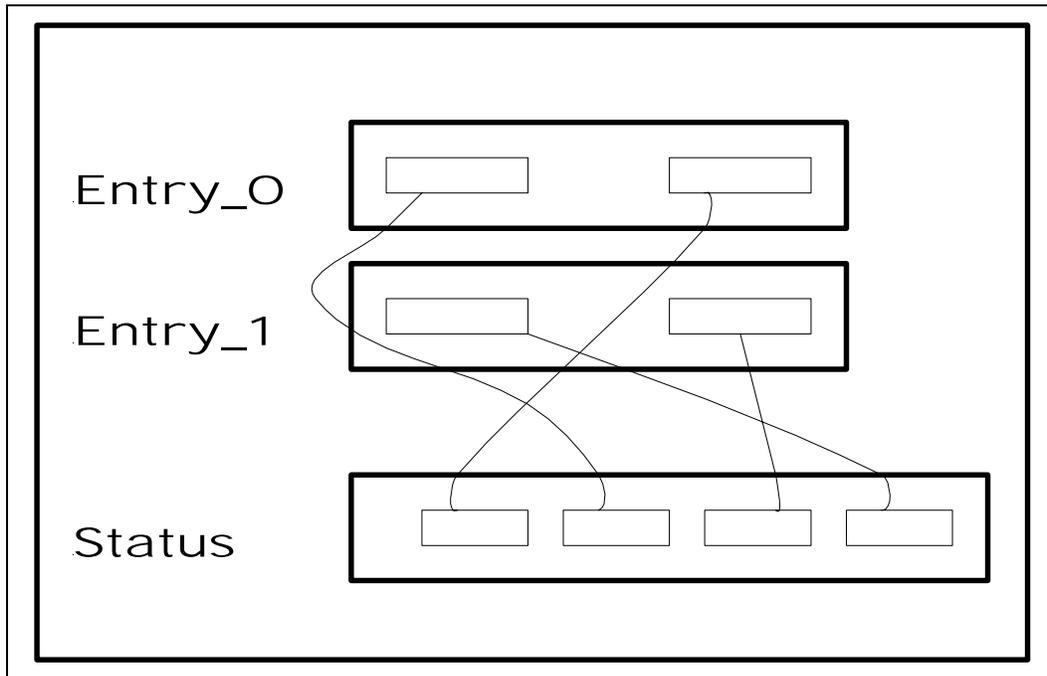
Entry_0 0x 0AAA AAAA
Entry_1 0x 0AAA AAAA (1010 reads back as 0101)
Status 5555 5550 5555 5550

(-3-26-01 current software version does not accept Msbit =1)

Entry_0 0x 1111 2222 (this example shows how the word order maps.)
Entry_1 0x 4444 8888
Status 4444 8888 1111 2222

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Figure 16-1. Status Word Wrapping



The status word sequence corresponds to : J6, J7, J8, J9 at the physical connectors

16.7.3 Board test procedure:

After visual inspection .Install 4 loopback plugs in J6-9. Leave J5 empty.

Plug in the board. Apply power to the rack.

Observe the RED LED extinguish and the Green LED illuminate.

Set S1 to 0xFF (switches 1-8 up)

Set S2 to 0x01 (switch1 down , 2-8 up)

Run SURM. It should recognize a 3700 manufacturer ID, a Model of 511, and assign a ULA of 01 to the board (assuming only one module in the rack).. There should be no error messages.

Set S1 to 0x0F (switches 1-4 up, 5-8 down)

Set S2 to 0x01 (switch1 down , 2-8 up)

Run SURM. It should recognize a 3700 manufacturer ID, a Model of 511, and assign a ULA of 15 to the board.. There should be no error messages.

If there is a problem , exit SURM and run the Signal Tech application in debug mode.

Verify ID = 3700

Verify Devtype = 65535 with all switches in the down position—or whatever is set at the switches

Verify Status= 65471

Verify offset= 65295

Otherwise run the Signal Tech application in normal mode.

A fresh board will show a NVM eeprom failure since the Eprom has never been set up.

SET NVM values as described above

Verify that the software reports the EEPROM is written and verified.

Write the bit patterns described above into entry locations and verify results at the status location.

Remove and replace each fuse one at a time- verify that the RED LED illuminates each time.

Rerun SURM and the Signal Tech app verify that the NVM is ok and the loopback signals still work.

The above procedure was used to test the 10 boards at Signal Technology.

17 Appendix Five – Glossary of Acronyms

Acronym	Meaning
ACM	Amplifier Control Module
ADC	Analog to Digital Converter
APT	Accelerator Production of Tritium
Beta (β)	An energy (or particle velocity) parameter for an accelerator
BNL	Brookhaven National Laboratory
c	The speed of light in a vacuum: 30 cm (a foot) per nanosecond.
CAD	Computer Aided Design/Drafting
CCL	Coupled Cavity LINAC
CDR	Critical Design Review
CLK	Clock
Coax/Heliac	Coaxial cable – Heliac is a coaxial cable made by Andrew Corp.
CPLD	Complex Programmable Logic Device. A general-purpose logic chip that can be programmed to execute firmware.
DAC	Digital to Analog Converter
DSP	Digital Signal Processing. A microprocessor optimized for real-time signal processing.
DTL	Drift Tube LINAC
ECAD	Electronic CAD – schematic capture and PWB design
ECL	Emitter Coupled Logic: -5.2V logic family
ECLTRG	ECL Local Trigger bus (high speed, user definable) on the VXIbus P2 connector.
EPICS	Experimental Physics and Industrial Control System language. The LANL accelerator control system computer language.
FAULT_L*	Left backplane fault (internal RF fault signal for the RFCS)
FAULT_L/R*	Generic backplane fault (internal RF fault signal for the RFCS)
FAULT_R*	Right backplane fault (internal RF fault signal for the RFCS)
FDR	Final Design Review
FOARC	Fiber Optic Arc Detector. A system that uses fiber optics to detect the light emitted from waveguide arcs to trigger a fault.
FRCM	Frequency/Resonance Control Module
HEBT	High Energy Beam Transport
Heliac	See Coax
HPM	High Power Protection Module
HPRF	High Power RF system
I and Q	In Phase and Quadrature data – a way of representing vector data in Cartesian (X,Y) coordinates.
I/O	Input/output
IF	Intermediate Frequency – for SNS it is 50 MHz.
IOC	A VXIbus crate Input/Output Controller – a single-slot computer.
KHz	Kilohertz (1 000 cycles per second)
LANL	Los Alamos National Laboratory
LBL	Lawrence Berkeley Laboratory
LBUS	12 bit Local Data Bus (TTL, user definable) on the VXI P2 connector.
LEDA	Low Energy Demonstration Accelerator
LINAC	Linear Accelerator
LO	Local Oscillator Frequency – for SNS it is either (805 – 50 = 352.5 MHz) or (805 – 50 = 755 MHz). This frequency is multiplied (mixed) with the RF carrier to yield the IF in a down-converter. This frequency is multiplied with the IF in the FRCM to yield the control RF carrier.
MHz	Megahertz (1 000 000 cycles per second)
MO	Master Oscillator. The source of all precision timing signals for the RFCS
MPS	Machine Protection System
NC	Normal (not super) Conducting
ORNL	Oak Ridge National Laboratory

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Acronym	Meaning
PCB	Printed Circuit Board – see PWB
PDR	Preliminary Design Review
P-I or P-I-D	Proportional – Integral – Derivative Controller. A control loop that generates a correction term based on the error between the actual value and the setpoint (proportional term), the integral of the error (integral term) and the slope of the error (differential term). In a P-I controller the “D” is zero.
PLL	Phase Locked Loop. A method of accurately generating one frequency from another, different one.
PWB	Printed Wiring Board – preferred over PCB because PCB has negative environmental connotations.
RCCS	Resonant Cavity Control System
RF	Radio Frequency
RF_FAULT*	The “outside world” RFCS fault signal to the MPS.
RFCS	Radio Frequency Control System
RFQ	Radio Frequency Quadrupole – a type of accelerator cavity
RTDL	Real Time Data Link: The Event Link data from the BNL timing card that provides the pulse-to-pulse machine operations commands.
SNS	National Spallation Neutron Source – a particle accelerator
SRF	Superconducting RF
TBD	To be determined – Unknown at this time.
TTL	Transistor-Transistor Logic: +5V compatible logic.
TTLTRG*	8 bit Local Trigger bus (TTL, user definable) on the VXI P2 connector. Generally implemented in negative logic (LOW = true).
TVS	Transient Voltage Suppressor – a fast avalanche diode to clip impulse noise spikes.
VME	VersaBus Module Extensions – an industry-standard modular chassis and computer interface.
VXI, VXIbus	VME Extensions for Instruments – an extension of the VME standard to modular instrumentation.
WBS	Work Breakdown Structure – a system of dividing large tasks into manageable subtasks – of grinding milestones into inch pebbles.

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