

LA-UR-02-5164

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Submitted to: 2003 IEEE Aerospace Conference
March 8-15, 2003
Big Sky, MT



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Reconfigurable Computing in Space: From Current Technology to Reconfigurable Systems-On-a-Chip

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The performance, in-system reprogrammability, flexibility, and reduced costs of SRAM-based FPGAs make them very interesting for high-speed, on-orbit data processing, but, because the current generation of radiation-tolerant SRAM-based FPGAs are derived directly from COTS versions of the chips, several issues must be dealt with for space, including SEU sensitivities, power consumption, thermal problems, and support logic. This paper will discuss Los Alamos National Laboratory's approach to using the Xilinx XQVR1000 FPGAs for on-orbit processing in the Cibola Flight Experiment (CFE) as well as the possibilities and challenges of using newer, system-on-a-reprogrammable-chip FPGAs, such as Virtex II Pro, in space-based reconfigurable computing.

The reconfigurable computing payload for CFE includes three processing boards, each having three radiation-tolerant Xilinx XQVR1000 FPGAs. The reconfigurable computing architecture for this project is intended for in-flight, real-time processing of two radio frequency channels, each producing 12-bit samples at 100 million samples/second. In this system, SEU disruptions in data path operations can be tolerated while disruptions in the control path are much less tolerable.

With this system in mind, LANL has developed an SEU management scheme with strategies for handling upsets in all of the FPGA resources known to be sensitive to radiation-induced SEUs. While mitigation schemes for many resources will be discussed, the paper will concentrate on SEU management strategies and tools developed at LANL for the configuration bitstream and "half latches".

To understand the behavior of specific designs under SEUs in the configuration bitstream, LANL and Brigham Young University have developed an SEU simulator using ISI's SLAAC1-V reconfigurable computing board. The simulator can inject single-bit upsets into a design's configuration bitstream to simulate SEUs and observe how these simulated SEUs affect the design's operation. Using fast partial configuration, the simulator can cover the entire bitstream of a Xilinx XQVR1000 FPGA, which has 6 million configuration bits, in about 30 minutes.

Instead of using a combination of TMR and configuration scrubbing for bitstream SEU mitigation, the approach developed for CFE uses minimal logic redundancy along with an SEU detection and correction scheme to handle bitstream SEUs. Though this approach allows some SEUs to affect less critical user logic, it requires considerably fewer FPGA resources than TMR and allows bitstream SEU rates to be monitored.

"Half latches", another class of SEU sensitive FPGA state elements, are used to provide logic constants in user FPGA designs but are not explicitly controlled by the configuration bitstream. Upsets in half latches cannot be detected by readback nor corrected via configuration repair or scrubbing---only a full reconfiguration can reliably restore their state. We have created a tool, called RadDRC, which can replace all critical half latches with more visible and correctable constant sources.

Lastly, in looking forward, this paper will briefly consider the possible benefits and risks of using reconfigurable system-on-a-chip FPGAs, such as the Virtex II Pro, for reconfigurable computing in space. The paper concludes with a summary of challenges for using reconfigurable computing in space and a summary of future research at LANL in this area.