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Title:	Production and performance of the silicon sensor and readout electronics for the PHENIX FVTX tracker
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Intended for:	Frontier Detectors for Frontier Physics

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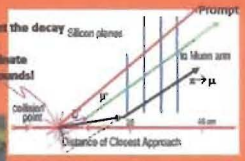
Production and Performance of the Silicon Sensor and Custom Readout Electronics for the PHENIX FVTX Tracker

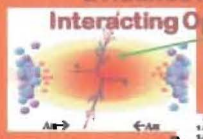
Jon S. Kapustinsky for the PHENIX - FVTX Collaboration

The Forward Silicon Vertex Tracker (FVTX) upgrade for the PHENIX detector at RHIC will extend the vertex capability of the central PHENIX Silicon Vertex Tracker (VTX) to forward and backward rapidities, (η), and also extend the reach in the low momentum-fraction region, (x). The FVTX is designed with adequate spatial resolution to separate decay muons coming from the relatively long-lived heavy quark mesons (Charm and Beauty), from prompt particles and the longer-lived pion and kaon decays that originate at the primary collision vertex. These heavy quarks can be used to probe the high density medium that is formed in Au+Au collisions at RHIC. The FVTX will also be used to study the spin structure of the proton.

Endcap detects the following by displaced vertex (Δr, Δz) of muons:



Evidence for Strongly Interacting Opaque Plasma

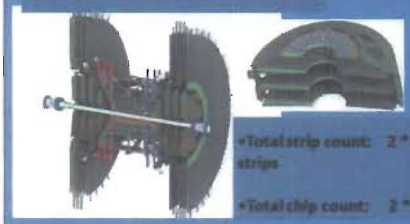


Energetic quarks undergo ... in the QGP

Data – PHENIX
Predictions – Vitev

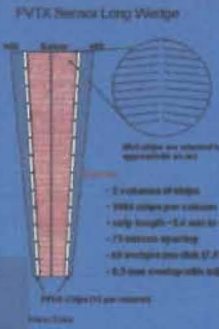
Absence of QGP effect of pions from Au+Au versus p+p and d+Au collisions

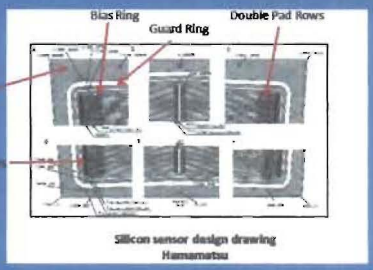
- Four stations of disks on each side
- One small disk (~60mm) three large disks (~126mm)
- Mini-strips of 75 micron radial pitch: 3.45 -11.2mm



- Total strip count: 2 * 552,960 strips
- Total chip count: 2 * 4320 chips

FVTX Sensor Long Wedge





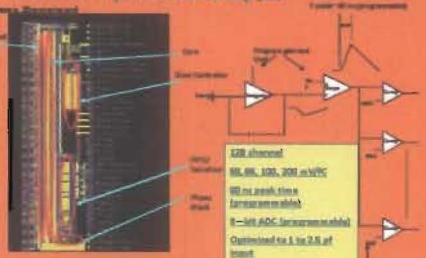
Silicon sensor design drawing
Hamamatsu

Silicon Wedge in an Assembly Jig

Detail – Probe and bond pads, guard rings on silicon sensor and input pads on the FPHX chip

Each endcap is comprised of four silicon disks covering opening angles from 10 to 35 degrees to match the existing muon arm acceptance. Each plane consists of p-on-n, silicon wedges, with ac-coupled mini-strips on 75μm radial pitch and projective length in the phi direction that increases with radius.

FPHX readout chip FNAL ASIC Group



128 channel
80, 85, 100, 200 mV/fC
60 ns peak time (programmable)
8—bit ADC (programmable)
Optimized to 1 to 2.5 pf input
115e + 13e/pf
~ 70 to 140 uW/ch (dep. Bias current)

Data push architecture
10 MHz beam clock (BCO)
200 MHz data clock
Zero suppressed
Output 4 hits/chip in one BCO
Approx. 302 uW/ch

A custom front-end chip, the FPHX, has been designed for the FVTX by the ASIC Design Group at Fermilab. The chip combines fast trigger capability with data push architecture in a low power design. The chip was fabricated in the TSMC 0.25 micron CMOS process

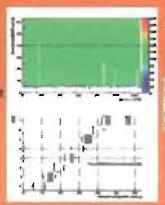
Photo of the FPHX

FVTX Wedge Assembly

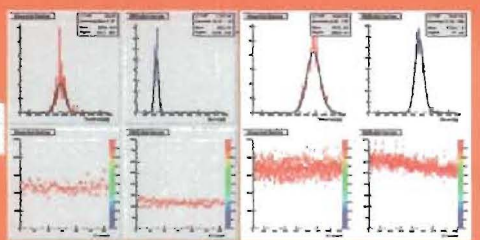
FPHX Prototype Test Results

Shaper output from pulse inject

Threshold turn-on curve



ADC linearity



Single Chip Performance

Integrated 13-chip Performance