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LA-UR-10-~~03574~~

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*Intended for:* 29th International Congress on High-Speed Imaging and Photonics, 20–24 September 2010,
Morioka, Japan

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Form 836 (7/06)

# Ultra-high speed burst-mode imager for multi-frame radiography

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**Abstract**
A 720×720 pixel hybrid-CMOS imager was fabricated by Rockwell Scientific (now Teledyne Imaging Sensors). Several cameras have been in operation for 5 years, in a variety of static and dynamic experiments, at the 800MeV proton radiography (pRAD) facility at the LANSCE accelerator. The cameras can operate with a per-pulse adjustable inter-frame time of 250ns to 2s, and with an exposure/integration-time as short as 150 ns. Given the 80 ms total readout time, the imager can be externally synchronized to 0.1-to-5Hz, 50-ns wide proton beam pulses, and record 1000-frame radiographic movies of 5-to-30 minute duration. The effectiveness and dependence of the global electronic shutter on the pixelated Si photo-sensor bias voltage is discussed. The spatial resolution dependence of the full imaging system on various monolithic and structured scintillators is presented. We also present features of a new-generation 10-frame, 1024×1024 pixel, 50-ns exposure, 12-bit dynamic range imager, which is now in the design phase.

Keywords: high-speed radiography, burst-rate MHz silicon-based imagers, fast imaging scintillators, performance of mega-frame/s rate cameras, global electronic shutter time behavior

## 1. Proton radiography - background

The high-resolution multi-frame dynamic proton radiography (pRAD) was invented at LANL in 1994 [1]. It was designed to record a large number of images (a radiographic movie) in a wide array of sub-microsecond scale (or longer duration) dynamic experiments. It has also been extensively used in static and tomographic imaging studies of various objects ranging from reactor fuel rods, or a combustion-engine block to pocket watches. The major advantage of proton radiography is its great penetrating power, especially at GeV energies, lower dose and background, multi-frame capability, ease of particle detection, as well as the mature proton accelerator technology. A few examples of recent work can be found in references [2] and [3]. Several other research institutions have either commissioned or are in the process of designing similar radiographic facilities [4].

At LANL the initial magnetic imaging system consisted of a set of proton-beam matching magnets and three pairs of image-forming magnetic lenses with the 1:1 magnification. The image of a radiographed object is formed on a 12×12cm mosaic of 2-mm thick LSO scintillator tiles. The images are recorded at two image stations (IL), located about 8m apart along the beam direction. Each image station was initially instrumented with single-frame EO-gated CCD cameras. The rapid shuttering of the CCD is accomplished via application of a 350 ns wide 10 kV pulse to a proximity-focused planar-diode (PPD). The PPD diode is fiber-optically coupled to the front face of the CCD chip [5]. The detection quantum efficiency (DQE) of the system is about 0.4. This is due to the lens coupling inefficiency, the necessary demagnification in the system optics, and the low quantum efficiency (QE) of the planar-diode photo-cathode (~ 15%). For each time-frame/view a separate CCD-PPD assembly was required.

In contrast to x-ray radiography, the number of radiographic images can be very large (well into many hundreds) and is determined by the number of proton bursts delivered by the 800 MeV proton linear accelerator at LANSCE. The duration of each proton burst (a strobe pulse) can be individually adjusted from 25 to >100ns. However, the number of recorded images is limited by the number of available cameras and their recording capability. Prior to introduction of the 3-frame imagers, there were seven single-frame cameras at IL1, and four CCD-based cameras in addition to two lower-resolution 9-frame framing cameras at IL2. That gave pRAD a 28-frame total recording capability.
In recent years this multi-pulse imaging system has undergone significant evolution. In order to boost the spatial

resolution in the object plane, two permanent magnet based "microscopes," were developed - one with a magnification of ×2.7, and a ×7 magnifier. Another enhancement to the system came in the form of 3-frame, high QE, 3-to-4 MHz hybrid CMOS cameras. The new cameras made possible to achieve the DQE equal 1, and increased the total number of the recorded high-resolution frames at IL1 to 19.

## 2. Three-frame silicon photo-sensor / CMOS hybrid 3-MHz burst mode imager

### *2.1 Basic imager parameters*

The imager was built around a hybrid CMOS FPA. The image capture circuit has been described in detail earlier [6]. The hybrid imager consists of a pixilated sensor with 100% optical fill-factor, which was bump-bonded to a CMOS readout integrated chip (ROIC). The ROIC was fabricated in mixed mode 0.25 μm CMOS technology. It was originally designed as a two-side buttable 720×720 pixel hybrid. The resulting total die size of 21.85×21.43 mm filled the available CMOS reticle area. In principle four such hybrids could be tiled to obtain the desired 1440×1440 pixel count. However, the chip tiling process turned out to be rather involved and expensive. Also from the point of view of gaining physics insight, as well as the experimental data acquisition, it was more effective to build and operate more of the single-chip 0.5-Mpx cameras, rather than one or two high-resolution imagers. That approach provided more frames (views) of fast processes even if the spatial resolution was somewhat reduced. At the moment there are seven single-chip cameras available at the pRAD facility at LANSCE. Six of them are located at the first image location station (IL1). That image station provides higher magnetic-lens resolution. The "proton" spatial resolution at IL2 is degraded as a result of the multiple scattering of proton beam in the upstream vacuum windows, and chromatic aberrations in the beam transport system. The basic parameters of the imager are listed in Table 1. The numbers in parenthesis indicate imager settings, exceeding the nominal specification, at which the cameras were successfully operated in several more demanding experiments.

Table 1. Nominal detector performance parameters

| | |
|---|---|
| Number of frames | 3 |
| Inter-frame spacing | 350 ns (250ns) |
| Shortest integration time | 180 ns (130ns) |
| Pixel size | 26×26 $\mu m^2$ |
| System effective dynamic range | 11 bit |
| Saturation level (well depth) | >200 $ke^-$ |
| Imaging array size | 720 x 720 pixels |
| Optical fill-factor | 100% |
| Quantum efficiency at 415 nm | 84% (95%@ 500nm) |
| Array readout time | 26 ms per frame |

### *2.2 Pixelated fully-depleted photo-detector*

As mentioned previously, the hybrid FPA chip is composed of two components: the pixelated photo-detector array and the ROIC. The detector array is substancially more light-sensitive and responsive than monolithic APS-CMOS –type sensors. The large pixels and fully-depleted nature of the diode array results in good spatial resolution. The optical fill-factor is close to 100%, since the detector array operates in a backside-illuminated mode. The AR coating and the large, on the order of 100 μm, sensor depletion depth results in QE which is uniformly high (80% to 95%) from 400 nm to 850 nm. The peak quantum efficiency is at 95% at 500 nm. In our particular case, at the scintillator emission wavelength (~415 nm) the QE is 84%. In addition to optimizing QE, the detector design was customized to achieve the needed short rise time (< 20 ns), and to minimize a parasitic contributions to the integrating node capacitance. Each photo-diode in the detector pixel array is connected (on the sensor p+ side) to the pixel signal-processing circuitry in the ROIC through an array of over 0.5 million indium bumps a few μm in diameter.

### *2.3 Readout Integrated Circuit and the SoC*

The ROIC consists of a 720x726 active pixel array, an analog chain to process and read out pixel signals, digital logic to generate required clocks and strobes, bias generator to generate all the required biases, and an on-chip analog-to-digital converter (ADC). A source follower based front-end snapshot circuit, with true in-pixel correlated double sampling (CDS), is implemented at each pixel integration node. Another source follower buffers the integration node from three sets of sampling capacitors. The three sets of sampling capacitors allow for the in-pixel storage of three (consecutive) snapshots. Such a configuration helps to minimize cross-talk, since each stored sample is buffered and read out through

an independent path. The pixels are first reset to erase charge from the previous frame. However, on opening of the reset transistor, an offset voltage due to charge injection and switching noise "sampling kTC noise" is deposited on $C_{int}$. The CDS circuitry cancels most of the kTC reset-noise as well as a low frequency component of 1/f noise. In order to achieve the desired noise figures, large in-pixel storage and CDS capacitors were required. Those constraints on the optimal sizes for the capacitors, and an implementation to ensure an acceptable leakage rate, limited the design to only 3 signal sample capacitors within a 26 μm pixel.

The ROIC was designed using a system-on-chip (SoC) approach. The result is a highly integrated, virtually "self-sufficient" digital imager. The user only needs to provide power, external master clock and trigger signals (in burst mode). The chip sends out digital video data via an external CamLink interface. The imager requires dual (3.3V and 2.5V) power supplies, "high voltage" detector bias (~15V) and a few decoupling capacitors for the ADC internal references. Readout timing logic and biasing are generated on-chip and can be programmed through a serial interface. The FPA's are cooled by a single-stage thermoelectric cooler and are typically operated at 0°C.

*2.4 Modes of operation: burst (integrate and then read-out) and continuous video*

Two imaging modes (burst mode and continuous mode) are implemented, selectable through the serial interface.
In *burst mode*, the user defines the integration timing through an external TTL "trigger" input. Three external consecutive triggers store three images on-chip; the width of each trigger pulse defines the corresponding integration time. After the third pulse, the imager reads out the stored frames automatically.
In *continuous mode*, two sets of the in-pixel storage capacitors are used. While integration is performed on one capacitor set, the other capacitor set is used to read out the previous frame. The third set of capacitors is continuously reset and not used in this mode. The integration time is programmable from 1 row time up to a frame time using the serial interface. In this mode, the chip can achieve a frame rate of up to 65 frames per second. This mode is very useful in camera set-up and focusing.

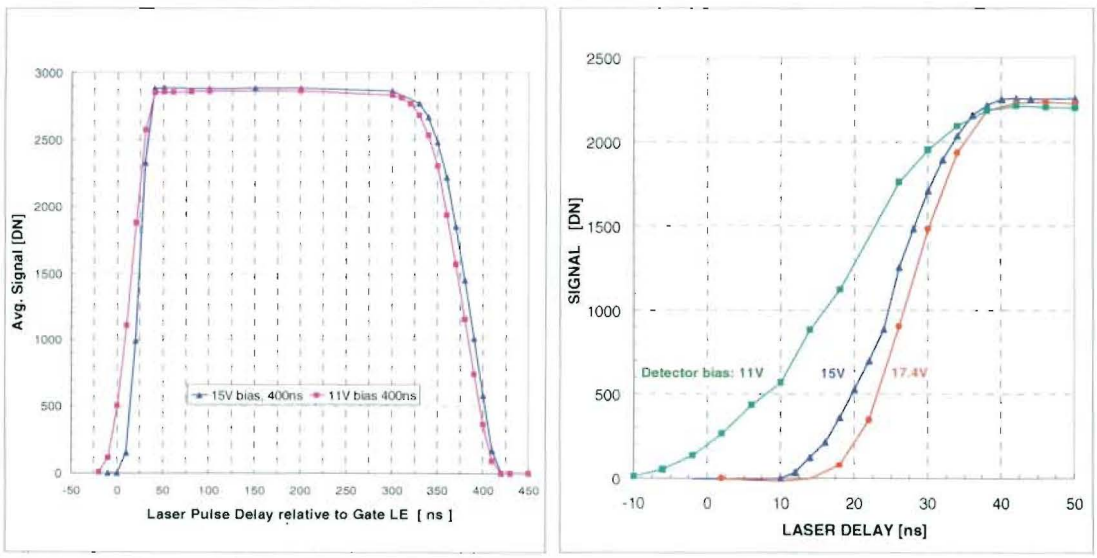


Fig. 1. Laser scans of 400 ns wide camera shutter-gate. Panel (a) shows the shutter turn-on phase, plateau response, and finally drop-off due to integration time effects and gate shut-off. Panel (b) illustrates strong dependence of the effective leading edge of the timing gate on the value of (fully depleted) photo-sensor bias. All data taken at 0 °C.

## 3. Camera critical parameter performance summary

*3.1 Shutter gate time definition and effectiveness*

The photo-sensor is a back illuminated pixel array of diodes implemented in n-type silicon. Since the absorption length in Si, for LSO generated 415nm light, is about 0.2 μm most of the electron-hole carriers are created close to the back surface (n+-side of the sensor), where the electric field is the weakest. Thus the dominant transport is that of the holes,

which drift to the p-n junction at the interface to the ROIC. The detector full depletion voltage is ~7.5V. The estimated transit time for the holes at room temperature and at the nominal bias of 15 V is 14.5ns. That transit time will affect the how well the leading edge of the shutter gate is defined. This is especially relevant if a light signal arrives just before the shutter "turn-on time."

In order to determine the performance of the camera shutter gates, and their dependence on the detector bias voltage we carried-out a laser pulse timing walkthroughs across the gates. The scans were done with a class 3A, 408 nm PicoQuant laser. The nominal width of the laser pulse was 50ps, however, but at high intensity it exhibits a small ~1ns long tail. The laser spot typically illuminated about ~80 pixels of the photo-sensor. The per-pixel amplitude of the pulse was adjusted so when the pulse was positioned within the time gate it produced a signal below the pixel saturation. At the start of the scan, a single laser pulse was fired at -100 ns before the arrival of a 400 ns wide shutter gate, and then the laser pulse was delayed in 50ns, or smaller steps, to "walk across" the three camera timing gates, one pulse per exposure time. The results of the scan for the first gate in the 3- trigger sequence are shown in Figure 1. The camera gates were

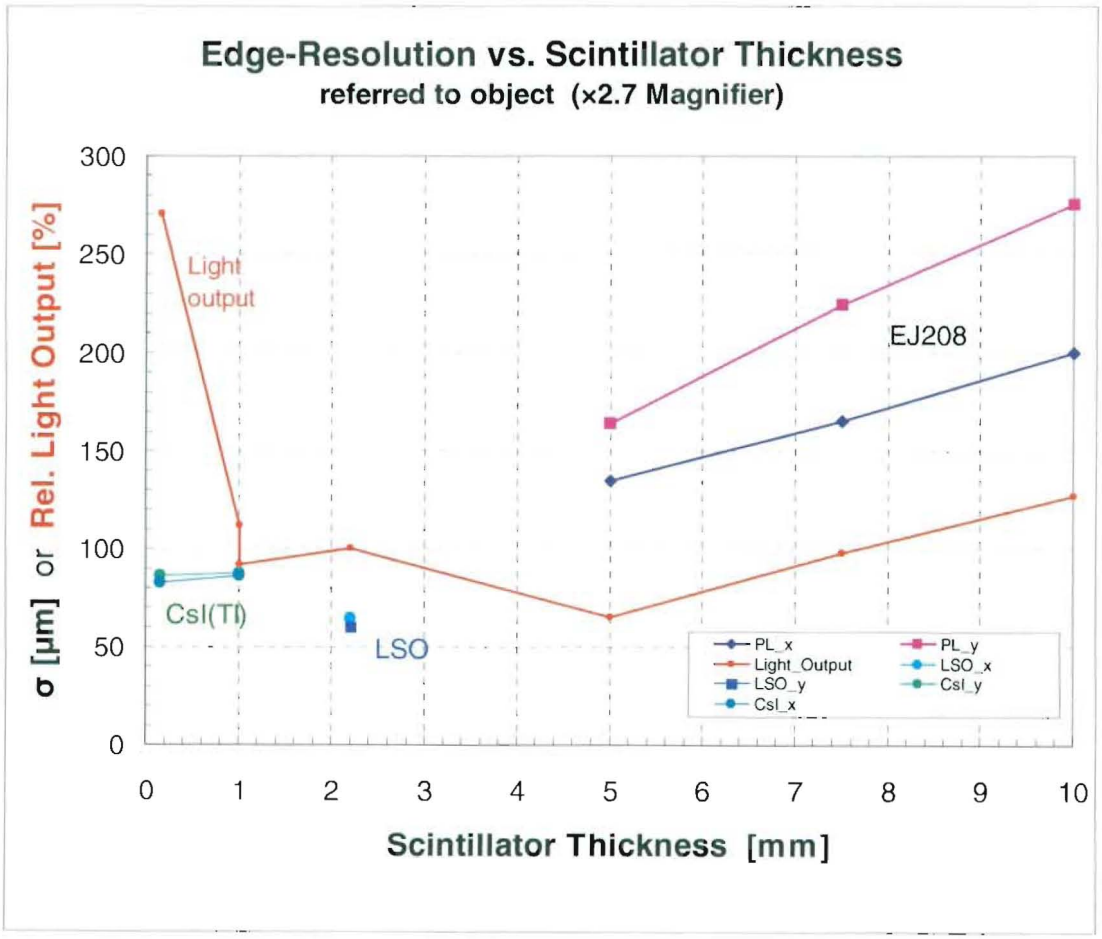


Fig. 2. System resolution of pRAD ×2.7 Magnifier (standard deviation 1-D Gaussian fit to a test object edges) plotted as a function of scintillator thickness. The thick red line shows the relative light output of the corresponding scintillator, normalized to 100% for 2.2 mm LSO. (A more conventional measure of resolution = 2.354*σ )

400 ns wide and 1 μs apart. At all the tested bias voltages the gate leading-edge response was wider than the expected carrier transit time through the depletion layer. However, the extinction ratio for pulses arriving at least 40 ns before the global shutter leading-edge, and after the falling edge is good >4000:1. The ratio is significantly better than what is observed in fast monolithic CMOS cameras, especially for the light signals arriving after the closing (often for 100's of

μs). This comes about because in the hybrid configuration, in which the relatively thick silicon detector acts as a light shield for the ROIC circuitry located underneath.

As shown in Fig. 1b the detector bias has a strong effect on the time spread/blurring of the leading edge of the shutter gate. The spread is wider than the values expected charge collection times at various voltages (16ns, 11.8 ns and 10.1 ns for 11V, 15, and 17.5 V bias). The ratio of the time spread to the theoretical transit time is not constant – it increases from 2.3, 2.4 to 3.2 as the voltage is lowered from 17.5V to 11V. This suggests some ns-long charge persistence at lower bias voltage, possibly due to e-h plasma cloud forming in a thin layer corresponding to maximum photon absorption. Some charge trapping may also occur in the Si bulk, due to detector radiation damage, or at the Si-$SiO_2$ interface may further contribute to the effect. At the nominal bias and with shutter gates set at >200ns those effects are relatively minor. However, in future hybrid CMOS imagers operating with shutter times $\leq$ 100ns one will have to use thinner, p-type detectors working at large over-depletion voltage and at lower temperatures.

### *3.2 Spatial resolution and dependence of system resolution on scintillator*

The camera field-of-view (FOV) on the imaging scintillator is adjusted from 15×15cm$^2$ down to ~10×10cm$^2$ depending on the needs of a current experiment. For a "typical" FOV of 13.2×13.2cm$^2$ the camera spatial resolution in the scintillator (or proton image plane), as tested with 400ns shutter gate imaging USAF target (at a demagnification of 7.1:1), was found to be 2.8 lp/mm, close to Nyquist limit of 0.184mm/px or 2.7 lp/mm. This can be compared to the standard deviation of a 1-D Gaussian fit to a differentiated sharp edge, which is used as quick first order estimate of the resolution, which gives a little optimistic value $\sigma_x$=142μm or FWHM =334μm. If taken at the face value it would yield 2.9 lp/mm in the scintillator plane. The resolution was weakly dependent on the sensor bias, unless the voltage was set below the full depletion. What is of more interest to the user is the effective resolution in the (radiographed) object plane. That effective system resolution is a convolution of contributions from three components: the proton-beam transport (mostly the magnetic lens and vacuum windows), scintillator and the camera. Taking the beam transport and camera contributions as constant, we scanned the dependence of the resolution on the type and thickness of the scintillator. The scintillators included: the standard 2.2 mm thick LSO $\tau$ = 42ns, fast $\tau$ = 2.3 ns EJ208 plastic scintillators 5-, 7.5- and 10-mm in thickness, and also 350 μm thick columnar- and 1 mm thick monolithic, $\tau$ = 1μs CsI(Tl). The figure 2 summarizes the results. One should keep in mind that some magnifier tunes can be optimized so that the resolution in one plane, say x, is better than that in the y direction. Clearly the LSO provided the best resolution $\sigma$ =65 μm, whereas the columnar CsI(Tl) offered the highest light output (×2.7 higher than 2.2mm LSO) with high-quality $\sigma$ = 83 μm resolution. The plastic scintillators can enable experiments, which need short inter-frame time intervals, however, at a non-trivial loss in the resolution and/or light output. Other basic camera parameters like the linearity, dark field behavior, sensitivity to stray radiation, charge holding time, etc will be addressed in a forthcoming paper.

## 4. New generation pRAD imager

Many dynamic basic physics and applied material science experiments at LANL need more and higher resolution frames, as well as shorter exposure and inter-frame time and higher dynamic range. Since it would be difficult to meet those demands with the present generation of 3-frame hybrid cameras, or other currently available commercial cameras we have under taken a new project to fabricate a new fast multi-frame imager. The CMOS ROIC chip is currently in the design stage. It will be implemented in 180 nm mix signal CMOS process. The parameters of the new and existing imagers are compared in the table below. The figure 3 on the right presents the layout of the 40 μm pixel with 10 signal-storage capacitors. To speed-up the read-out the chip is equipped with a single-ramp 13-bit ADC on a per column basis. The effective 12-bit dynamic range can be maintained across full range of shutter times. The large size of the ROIC chip (4.2×4.3cm$^2$) will necessitate CMOS stitching in the fabrication.

## 5. Conclusions

The first generation of the 3 MHz burst-mode hybrid pRAD cameras has been successfully operated in a moderate radiation environment for over 5 years. The imagers still shows good extinction ratio both in pre- and post-shutter time regimes. The leading edge of the effective shutter gate shows a time blur width of at least twice the carrier transit time through the sensor. The shutter-gate time definition issues will have to addressed in the future ns-shutter time hybrid CMOS imagers. As Moore's law is beginning to run into difficulties in the analog world of the single plane CMOS design, it is likely that the future development of high-performance imagers will proceed along 3-D CMOS interconnect

architecture [6-9]. The 3-D approach allows mixing various CMOS technologies to independently optimize the analog and digital functions, and most importantly for our applications it will permit to significantly increase the number of stored- or processed "on-the-fly" frames.

| Design Parameter | pRAD-1 Imager | pRAD-2 2nd Gen Imager |
|---|---|---|
| Minimum integration time (Global shutter) | 150 ns | **50** ns |
| Nominal min. inter-frame time | 350 ns | 150 ns |
| Effective Dynamic Range | 11.4 bits | 12 bits |
| Read noise | 100 e- | ~ 37 e- |
| Imaging array size | 720×720 px | 1024×1024 px |
| Number of samples/ frames | 3 | **10** |
| Pixel pitch | 26 μm | **40** μm |
| Sensor QE @ 415 nm | 84% | >90% |
| Chip dimensions | 21×22 $mm^2$ | **~42×43** $mm^2$ |
| Optical Fill-Factor | ~100 % | ~100 % |
| Saturation level/ Well depth | >200 $ke^-$ | ~ 150 $ke^-$ |

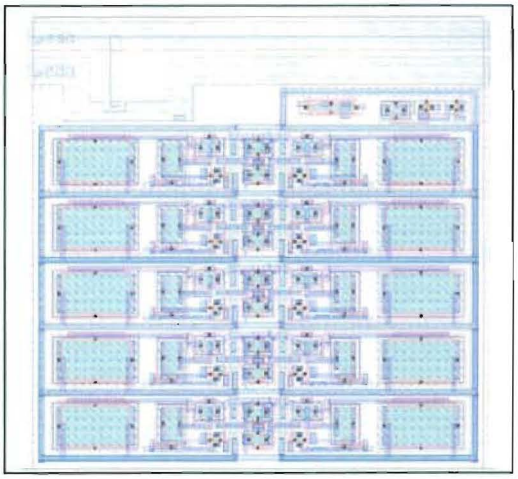

Fig. 3. Circuit layout of 40 μm pixel showing the location and packing of the 10 in-pixel signal-storage capacitors.


## Acknowledgments

This work was supported by the United States Department of Energy. The authors wish to thank Michael Lesser of University of Arizona, Zheng Li and Paul O'Connor of BNL, Henrik von der Lippe and Helmuth Spieler of LBNL for their contributions to the projects' CDR's.


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