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Title: A Proton Radiography Concept at NNSS (U)

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Form 836 (7/06)

Abstract for "A Proton Radiography Concept at NNSS"(U)

Experience in 800MeV dynamic proton radiography at the Los Alamos LANSCE facility coupled with a series of static measurements completed at the Brookhaven AGS at 24GeV/c have resulted in obtaining a good understanding of the anticipated performance of a facility tailored to meet future radiography requirements at the NNSS. This is to a large degree an update to a previous study completed in 2004 addressing the same topic.

A more complete analysis of the AGS data, a comparison of test object results between current x-ray and proton radiography capabilities, and more dynamic results relevant to scaling and surrogacy issues are included. Strong evidence is provided to indicate proton radiography can meet or exceed current radiographic requirements for a future facility in a timely and cost effective manner.

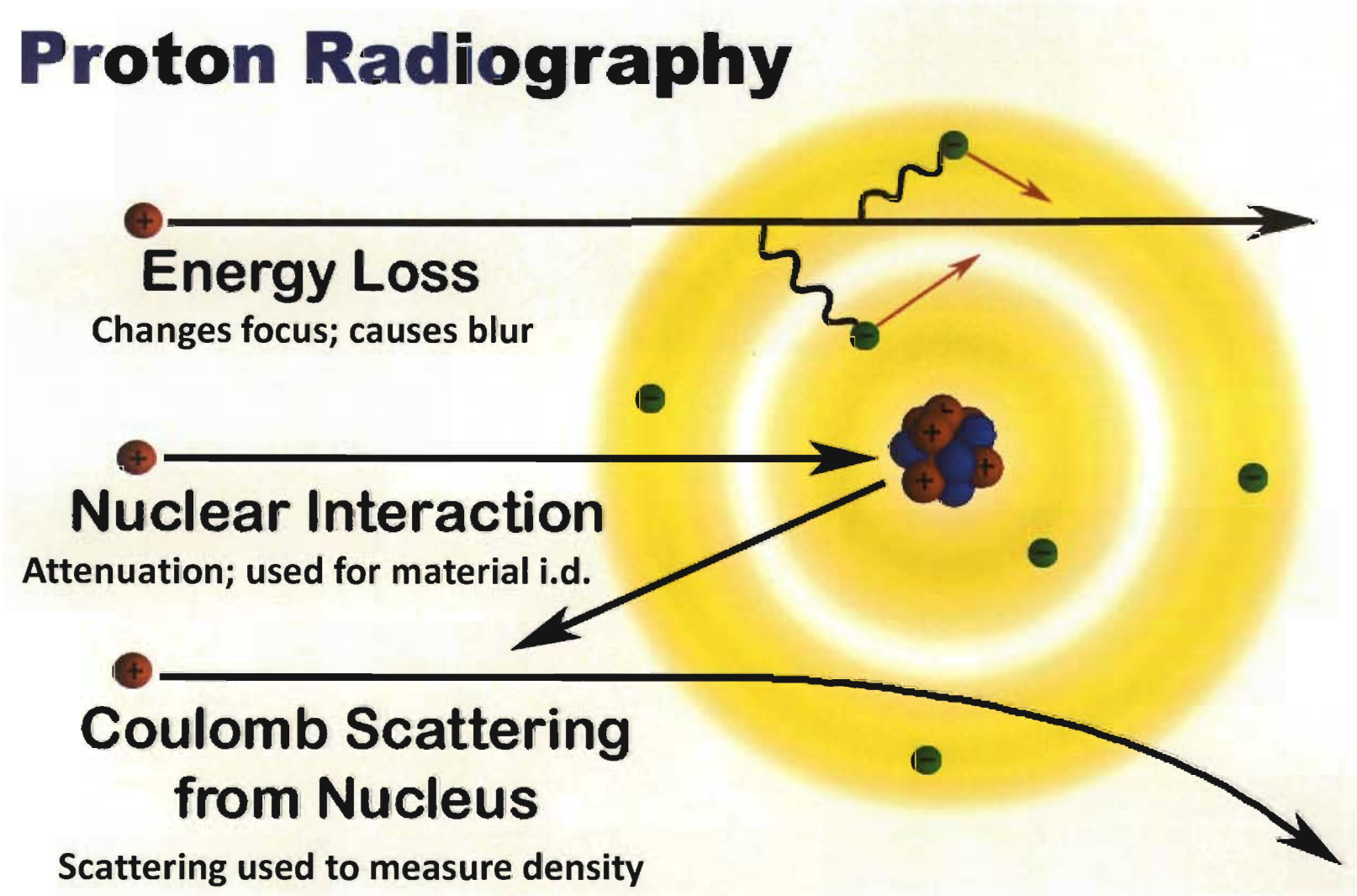
A Proton Radiography Concept at NNSS
Unclassified slides

Doug Fulton

Chris Morris, Kris Kwiatkowski, and Nick King

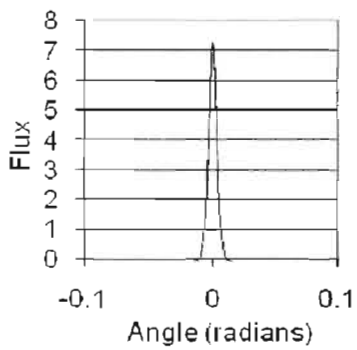
5/4/2011

Proton Interactions

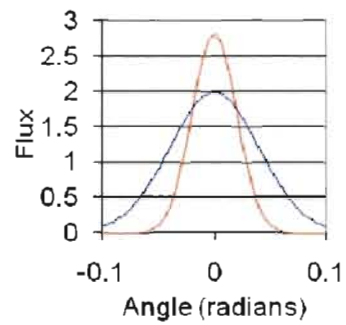


Contrast from Multiple Coulomb Scattering

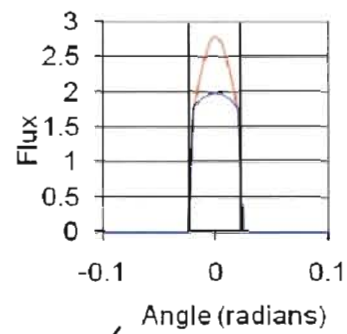
Incident Beam



After Object

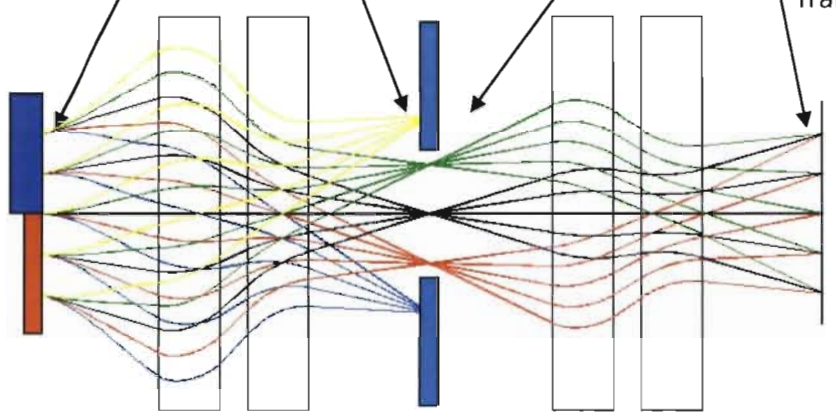


After Collimator

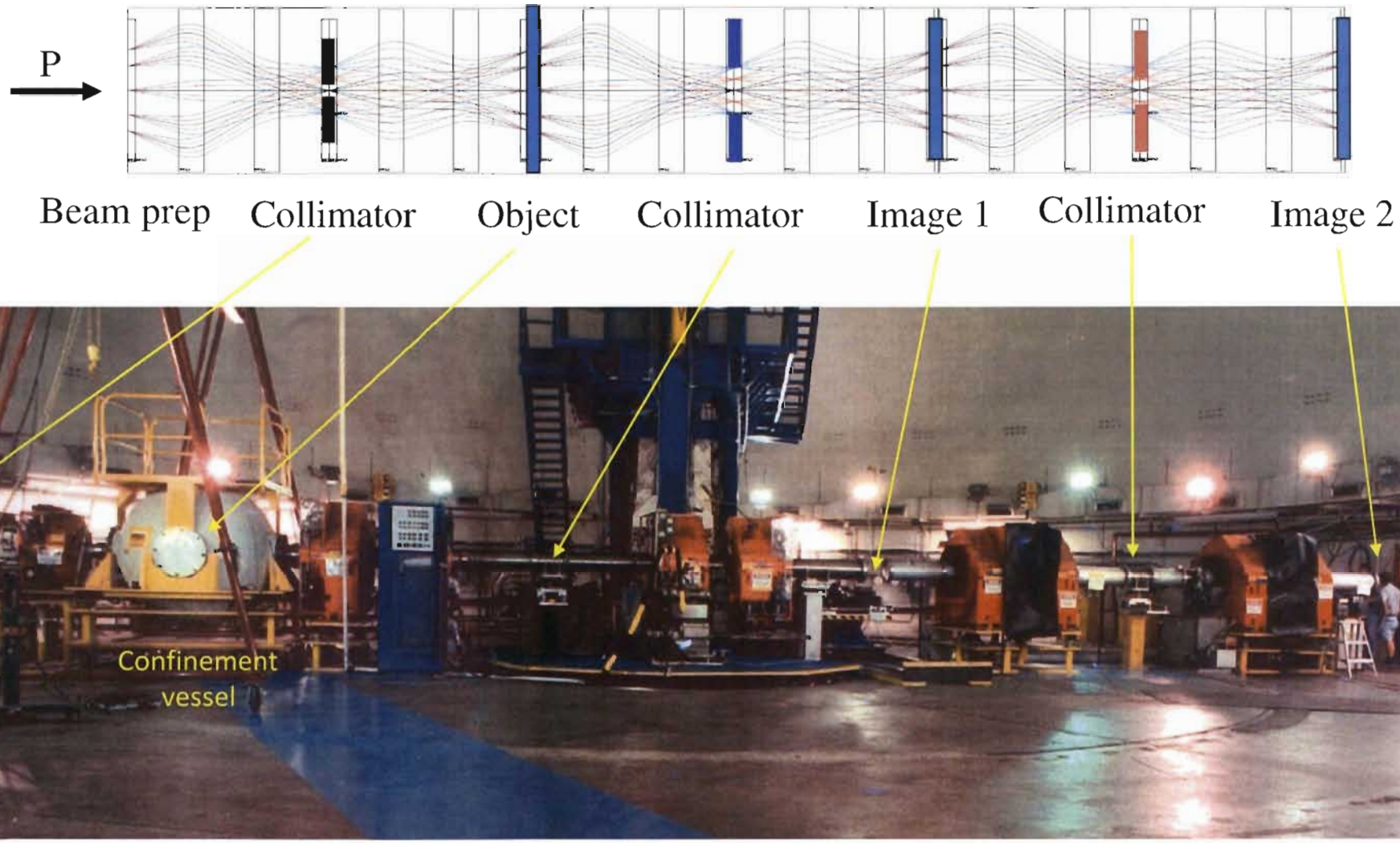


Measured transmission provides information of object thickness

$$T = e^{-x/\lambda}\left(1 - e^{-\left(\frac{\theta_c p\beta}{14.1\,MeV}\right)^2 \frac{x_0}{2x}}\right)$$

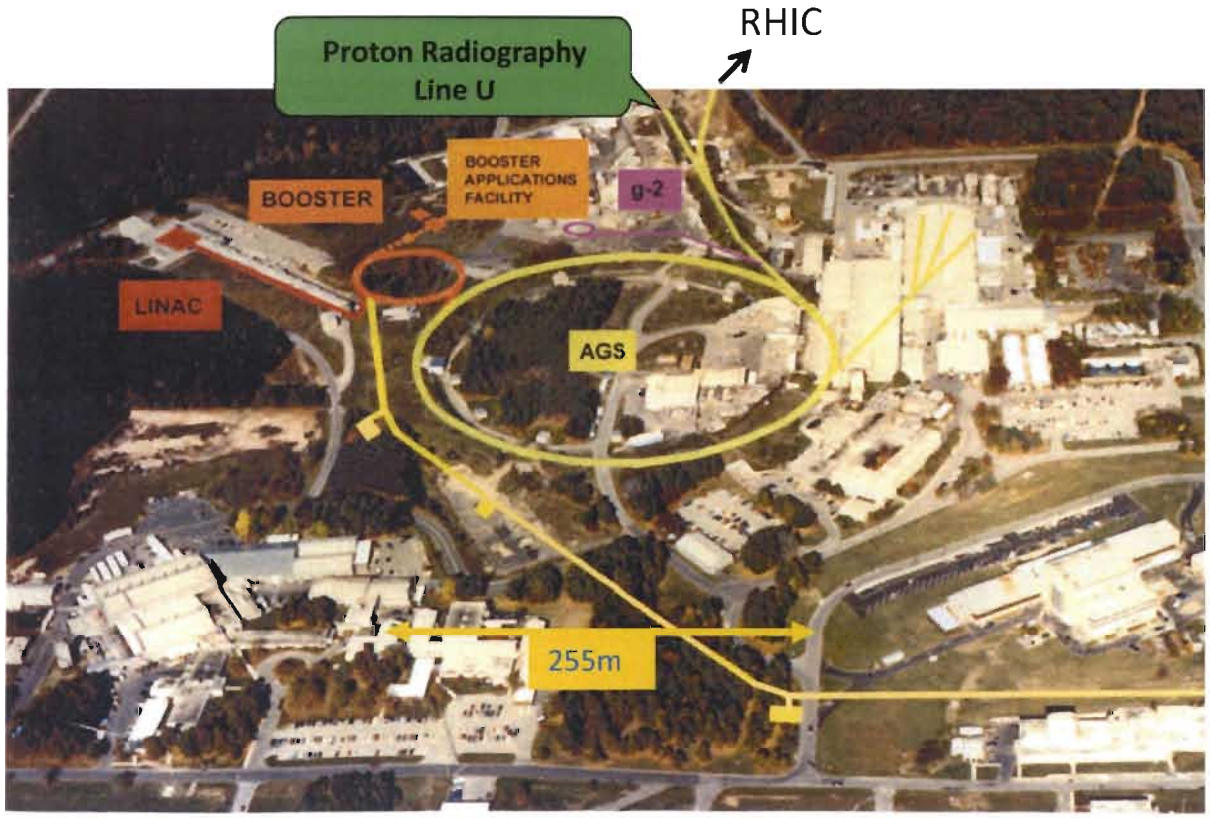


LANSCE 800 MeV proton radiography facility (U).



An example of the concept at BNL/AGS

AGS accelerator at Brookhaven



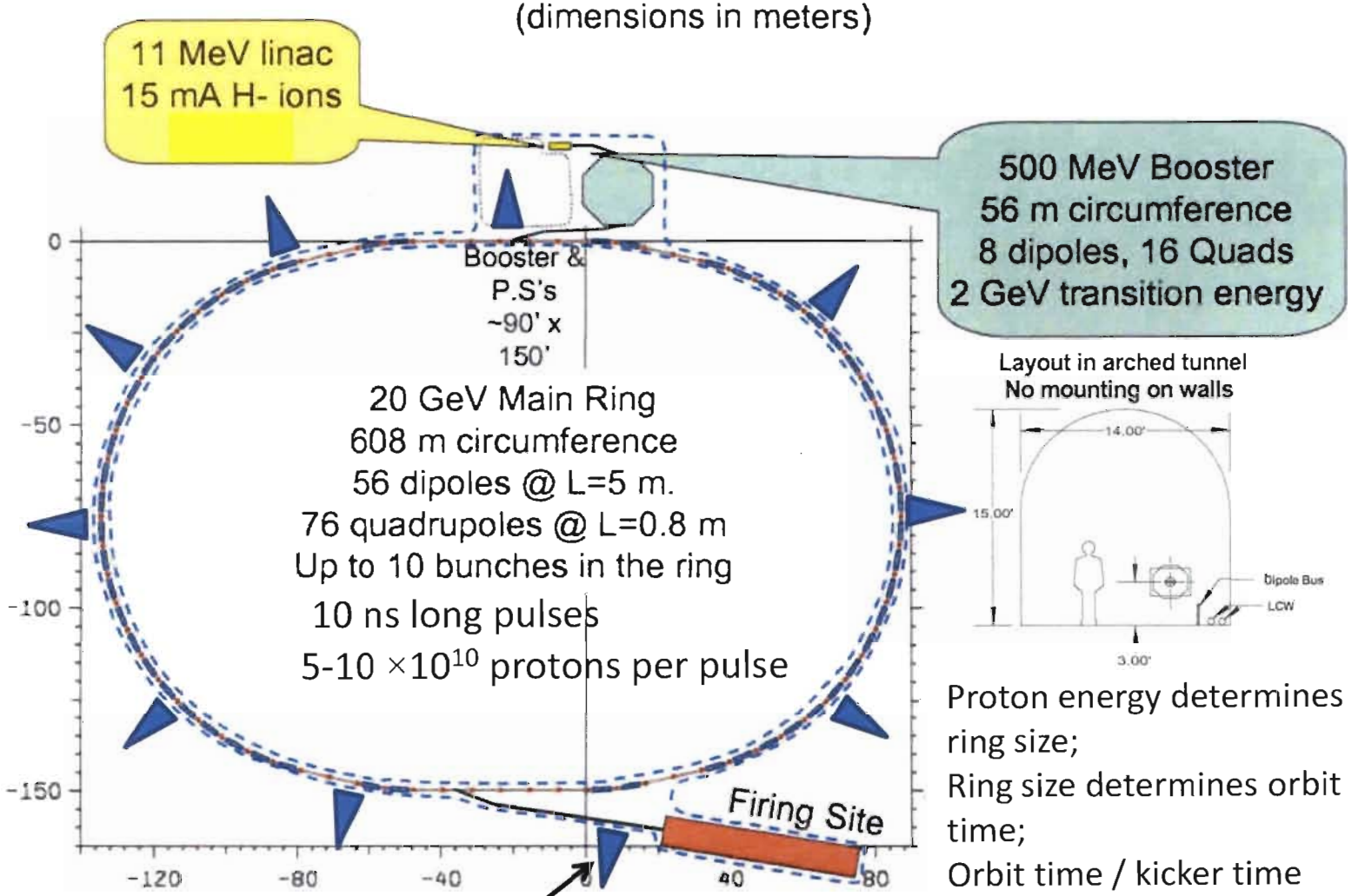
Line U

24 GeV/c protons
30 ns long pulses
5×10^{10} protons per pulse

pRad magnetic imaging lens system in Line U Tunnel

Schematic Layout of Accelerators

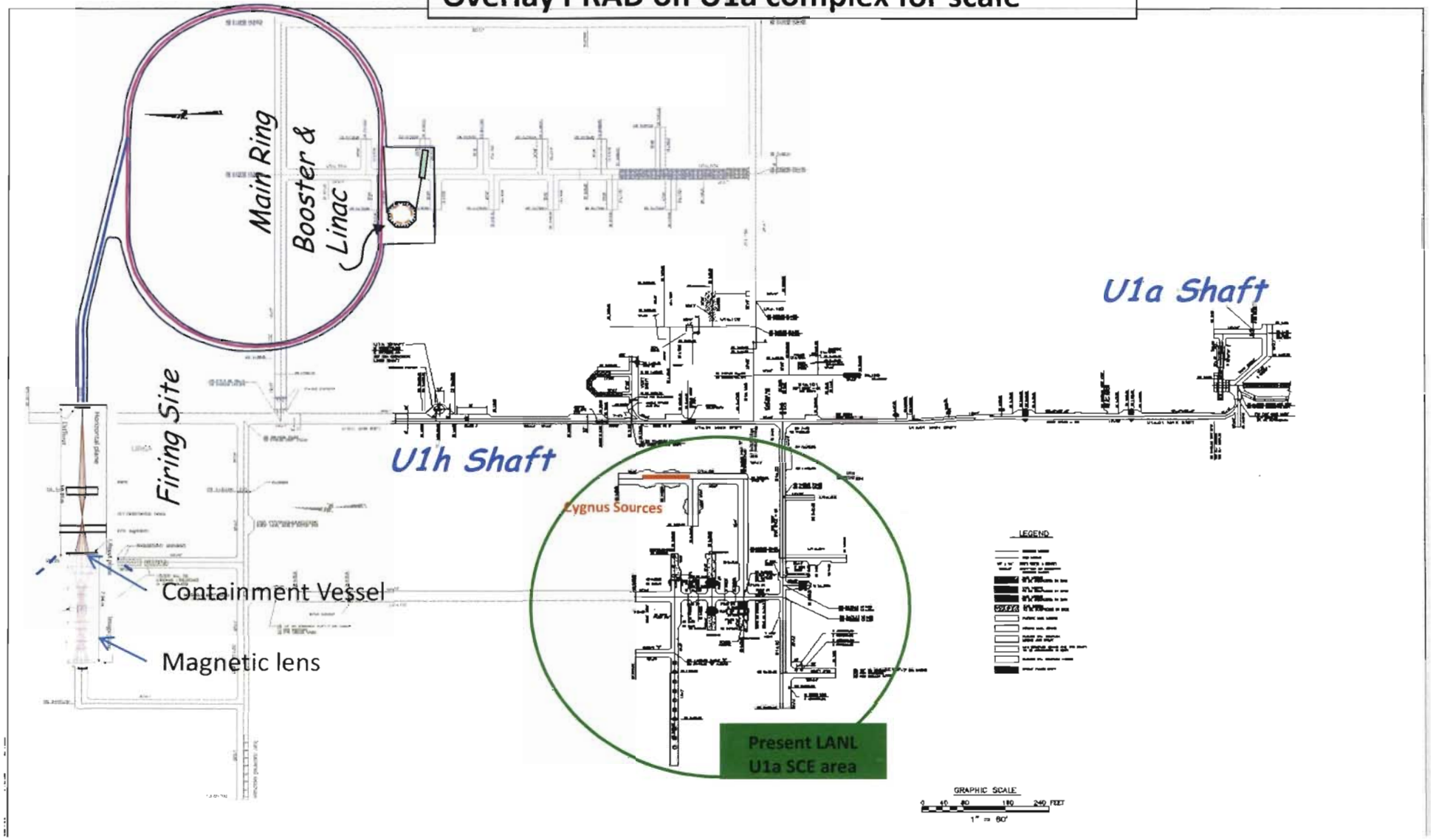
(dimensions in meters)



Proton energy determines ring size;
Ring size determines orbit time;
Orbit time / kicker time determines # of pulses

Notional proton pulse exiting ring

Overlay PRAD on U1a complex for scale

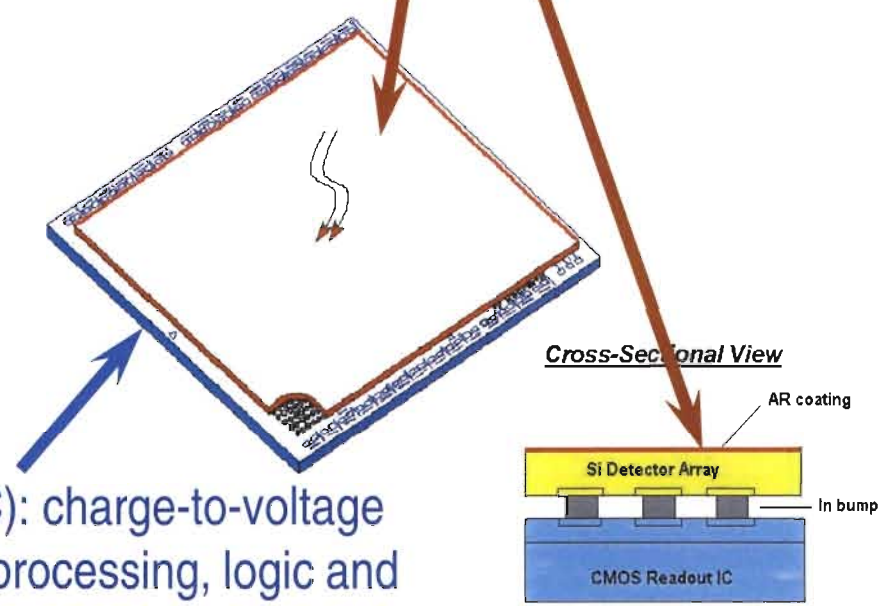


Detector Technology: Two-Component CMOS-Hybrid

- Independent optimization of detector and readout IC
- QE -84-95% (400-900 nm), ~100% optical fill factor
- Fast 150ns CMOS shutter, 250 ns inter-frame time
- Excellent extinction ratio; 3-frame in pixel storage

(1) Photo-Sensor Pixel Array (photon-charge conversion)

- 7 cameras (720×720 px) built & in use since 2005 (prototype $1.16M)
- 2nd gen (1100×1100 px) in design stage



(2) CMOS Readout IC (ROIC): charge-to-voltage conversion, signal storage & processing, logic and A/D conversion

System on Chip: photons-to-bits

Existing vs. 2nd Gen CMOS Hybrid Imager

We are evaluating the use of the 2nd generation imager on DARHT

Design Parameter	pRAD-1 Imager	New 2nd Generation pRAD Imager
Minimum integration time (Global shutter)	150 ns	50ns
Nominal min. inter-frame time	358 ns	150 ns
Effective Dynamic Range	11.4 bits	12 bits
Read noise	100 e-	~ 35 e-
Imaging array size	720×720 px	1100×1100 pixels
Number of frames	3	10
Pixel pitch	26 μm	40 μm
Sensor QE @ 415 nm	>80%	>90%
Chip size	21×22 mm^2	~44×45 mm^2
Optical Fill Factor	~100 %	~100 %
Saturation level/ Well depth	180 ke-	~ 150 ke-

Reducing the Risks

Low risk – demonstrated technology
Medium risk – modification of existing technology
High risk – new technology

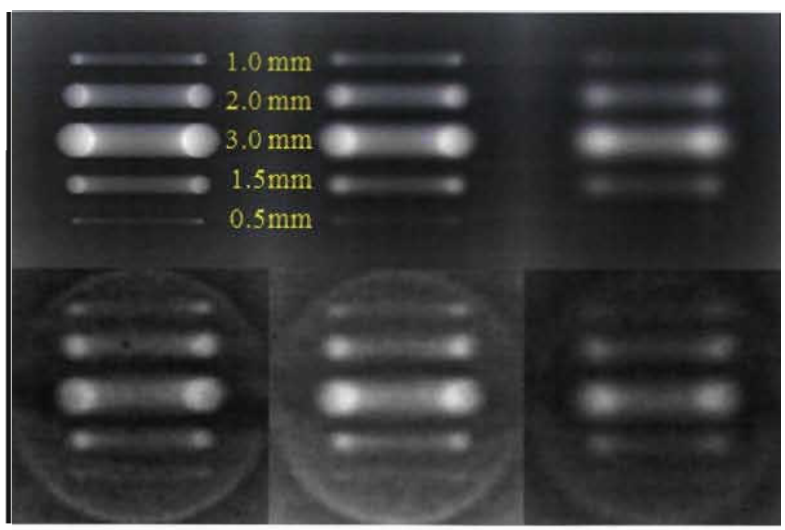
	Containment	Kicker	Cameras	Analysis
Level	medium	low/medium	low/medium	low
Consequence	>100 µm point spread function	200 ns minimum spacing	200 ns minimum spacing	Less accurate density reconstructions
Development plan	Build classified beam line at BNL/AGS to test window designs	Build and test kicker at BNL/AGS; move to NNSS	Complete existing camera designs / build plan	Implement pRad physics into BIE
Cost by FY FY12 / FY13			$2M / $2M	$0.75M / $0.75M

Window 80 cm from Object (window resolution is inversely proportion to window radius)

No window σ=0.01 | 2.5 cm Aluminum σ=0.027 cm | 2.5 cm Steel σ=0.061cm

Model

Data



We believe the schedule risk continues to be high.

Backup

pRAD-2 10-frame imager for 800MeV pRAD at LANSCE – Project Status

2nd gen CMOS-hybrid: 10-frame capability, improved resolution (1.2Mpx), excellent QE, 50ns shutter, good radiation resistance

- Total estimated cost of prototype development $3.5M (two camera systems will be delivered)

- As of April-2011, CMOS readout chip (ROIC) design is 90% completed; $160k to finished (funded, PO to Teledyne underway)

- Next step: ROIC chip fabrication - min. needs 10-wafer CMOS run at TowerJazz Semiconductor; then testing (TIS). Partially funded (PR in purchasing) - $417k and $271k; needs additional $270k for second CMOS run and automated wafer probing

- Funding for FY12 to complete the project: $2M (will cover: pixelated photo-sensor fabrication, bump-bonding to ROIC, digital logic controller, dewar, TEC cooling, lenses, acquisition software,...). *Does not include any contingency.*