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HARDWARE DESCRIPTION ADSP-21020 40-BIT FLOATING POINT DSP AS DESIGNED IN A REMOTELY CONTROLLED DIGITAL CW DOPPLER RADAR

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Abstract

A continuous wave Doppler radar system has been designed which is portable, easily deployed, and remotely controlled. The heart of this system is a DSP/control board using Analog Devices ADSP-21020 40-bit floating point digital signal processor (DSP) microprocessor. Two 18-bit audio A/D convertors provide digital input to the DSP/controller board for near real time target detection. Program memory for the DSP is dual ported with an Intel 87C51 microcontroller allowing DSP code to be up-loaded or down-loaded from a central controlling computer. The 87C51 provides overall system control for the remote radar and includes a time-of-day/day-of-year real time clock, system identification (ID) switches, and input/output (I/O) expansion by an Intel 82C55 I/O expander.

I. Introduction

In 1985, staff members of Los Alamos National Laboratory began a program to build a CW Doppler radar that could be used as a tool for collecting metrological data such as tornadoes, funnel clouds, and wall clouds. The radar was designed to be used in the field at or near ground level and to have an operating range of up to 10 km.

The result of the effort was the development of a low power, portable, continuous wave (CW), 3-cm (10GHz) Doppler radar[1]. The system was fully analog and data was recorded on a high quality audio tape recorder. This data would then be returned to the laboratory where it would be digitized for analysis. The radar performed very well during field testing in 1987 and 1988[2].

Following the successful operation of the all analog radar, a new effort was started in 1987 to further develop the system. A major new objective for this effort was to develop a system which could be deployed into the field and operate unattended for long periods of time. Remote monitoring and data retrieval would then take place over a standard RS232 data link from a central location. To satisfy this objective the radar was redesigned with digital signal processing and analysis capabilities on board. The system used 14 bit Analog-to-Digital converters (ADCs) and

an Analog Devices ADSP-2100 16-bit, fixed point DSP. Initial testing of the radar was very encouraging. Unfortunately the program was stopped at the prototype stage for non-technical considerations. The ADSP-2100 has since found its way into numerous applications ranging from filters to image processing to sonar detection[3]. This paper will describe the hardware portion of the DSP/controller board. A discription of the RF and DSP software of the system is given by Robinson and Morrison.[4]

In 1991, the program was restarted and the system was redesigned to incorporate recent advances in DSP, ADC, and microwave hardware. Current objectives of the program include increasing the radar's detection and reporting capabilities, improvement of its packaging to better support field deployment, and remote operation; and to provide for future system growth.

II. System Description

The system consist of a host personal computer (PC) and a remote radar unit. The remote radar system consists of an RF unit, the DSP/controller board, and a power supply. The RF unit contains power converters, microwave source and amplifier, quadrature mixer, transmit and receive antennas, and signal amplifiers. The heart of the system is a dual processor DSP/controller board located in the remote radar unit. The processors used are the Intel 87C51 microcontroller and the Analog Devices ADSP-21020 DSP[5].

Figure 1 is a block diagram of the DSP/controller board. The ADSP-21020 is based on a Harvard architecture; thus separate address and data busses are provided for both program and data memory. Data bus width is 40-bits for data memory and 48-bits for program memory. The address bus is 32-bits for data memory and 24-bits for program memory. Two bank select lines are available for program memory and four bank select lines are available for data memory. These select lines are user programmable.

An analog to digital (A/D) converter and a digital to analog (D/A) converter are attached to the data memory side of the ADSP-21020. Two input channels (Figure 2) from the RF unit are connected to the A/D converter. Digitized output from the A/D (Figure 3) is connected to two electrically programable logic devices (EPLD) and then connected to the ADSP-21020 data bus. An expansion connector is provided for a D/A converter that can be piggy-backed onto the DSP/controller board. This connector provides data and control lines and is used primarily for diagnostics during the development stage. However, any device can be attached to the expansion connector. The A/D, shown in figure 3, and the D/A are mapped into separate memory banks by using the data memory select lines.

There are two analog input channels on the DSP/controller board from the RF section; the I and Q channel outputs from the quadrature mixer. Only one stage of amplification is provided on the DSP/controller board as signal amplifiers and line drivers are placed in the RF section. The two analog signals are connected to a Crystal CS5128 stereo A/D converter. The CS5128 is an

18-bit dual channel Delta-Sigma converter with built-in digital anti-alias filtering, sample and hold, and voltage reference. A summary of the specification for the CS5328 is shown in Table I.

TABLE I
SPECIFICATIONS FOR THE CS5328 A/D CONVERTER

Dynamic range.	97 dB
Signal-to-noise (+ distortion) . . .	94.5 dB
Total harmonic distortion	0.00015%
Internal oversampling .	64X
Passband ripple . . .	0.001 dB
Stopband rejection . . .	86 dB
Interchannel phase deviation. . .	0.001 degrees
Interchannel isolation (DC to 20 kHz). . . .	106 dB
Power dissipation	
active	450 mW
standby	20 mW

After dividing internally, a 6.54 MHz clock provides for a 50.4 KHz sampling rate on each of the A/D input channels. Data is output from the A/D on a serial line. Two Altera EPLDs, EP610C-35XD, perform serial to parallel conversion and the appropriate clocking and latching interface from the A/D to the ADSP-21020 DSP data memory bus. An end-of-conversion interrupt signal is generated by the EPLDs and tied to the ADSP-21020 IRQ1 and IRQ2 interrupt input lines. Thus the ADSP-21020 is acquiring one channel of 18-bit A/D data approximately every 19 milliseconds.

Data memory consists of 32K x 40 bit static RAM consisting of five Integrated Device Technology 256K x 8 bit devices (IDT71256L-25), and is shown in Figure 4. The ADSP-21020 has four data memory select lines. One line is used to select the data memory static RAM, another line is used to select the A/D converter, and a third line is used to select the expansion connector. The data select lines allowed for a simplified memory design in that the functional areas (RAM, A/D, and D/A) could be placed in separate memory banks. Although the ADSP-21020 has 32 data memory address lines, 32K of data memory was deemed more than adequate for this application.

Program memory for the ADSP-21020 is 48-bits wide, as shown in Figure 5, and is configured as 32K x 48-bit. This memory consists of 6 IDT71256L-25 static RAMs. Program memory is dual-ported with the 8-bit 87C51 microcontroller. Address, data, and control lines from the ADSP-21020 and the 87C51 are tied to discrete logic gates, buffers, latches, and another Altera EPLD (EP610C-35XD) which provide for access control to the ADSP-21020 program memory as shown in figure 6.

As the 87C51 can only address 64K of 8-bit external data memory, two lines of port 2 on the 87C51 are used as external data memory bank select lines. This allows the 87C51 to address the full 32K x 48-bit of ADSP-21020 program memory by having three separate 64K x 8 external data memory banks. Figure 7 is a schematic of the 87C51 logic and provides details of the memory map of the 87C51. The 87C51 exercises control of the ADSP-21020, shown in figure 8, by controlling the RESET and BUS

REQUEST lines of the ADSP-21020 via separate lines on port 2.

Mapped into the 87C51 external memory space, external data memory bank four are: ID select switches, used to manually configure multiple remote radar stations: a Dallas Semiconductor DS1287 time-of-day/Day-of-year real time clock; and an Intel 82C55 I/O expander. A connector is provided for the I/O expander allowing a piggy-back board to be attached to the DSP/controller board. This board is intended to be used for an 8-bit A/D converter which will monitor system parameters such as battery voltage, RF power, and temperature, and to provide for future system expansion. Serial transmit and receive lines from port 3 of the 87C51, and three other port 3 lines are connected to a MAXIM MAX 235 RS232 signal translator chip to provide communications with the host PC using an RS232 data line.

III. System Operation

When the system is first powered on, the 87C51 resets devices by way of the RESET line and powers down the RF unit power converters by way of the RFPWRDN line. Separate I/O lines on port 2 of the 87C51 are used for this purpose. Another I/O line on port 2 is used to assert the bus request, BR, line to the ADSP-21020; thus the ADSP-21020 is forced into an idle state in which address, data, and control lines are tri-stated. The 87C51 then goes into a loop waiting for a command from the host computer.

One of the host computer commands is to down-load data to the remote radar unit. This data is actually object code created using Analog Devices software development tools for the IBM PC. A software utility developed at Los Alamos National Laboratory reformats this object code so that it can be sent in packets from the PC to the remote radar. Transmitted data is loaded into the ADSP-21020 program memory.

Another command from the host computer instructs the remote radar to turn on; in addition to 100% operation the PC can instruct the remote radar to operate on a duty cycle basis. Once the remote radar is enabled, the 87C51 releases the BR line to the ADSP-21020, which in turn disables the 87C51 access to program memory and causes the ADSP-21020 to start program execution from address zero of program memory.

The ADSP-21020 signals the 87C51 when a detection is made by raising the FLAG0 line. This line is tied to the 87C51 interrupt pin INT0. The 87C51 asserts BR to the ADSP-21020, waits for the BG response, then reads detection data from the ADSP-21020 program memory. This data is then transmitted to the host computer. The host PC acknowledges receipt of the data. The 87C51 then returns control to the ADSP-21020. If the host PC does not acknowledge receipt of the data, the 87C51, after an appropriate time-out period, logs the data in a software created first-in-first-out (FIFO) buffer. This data will be transmitted as soon as a link is established.

The ability to duty cycle operation of the remote radar allows for power savings at the remote site. When the ADSP-21020 and A/D are in an idle

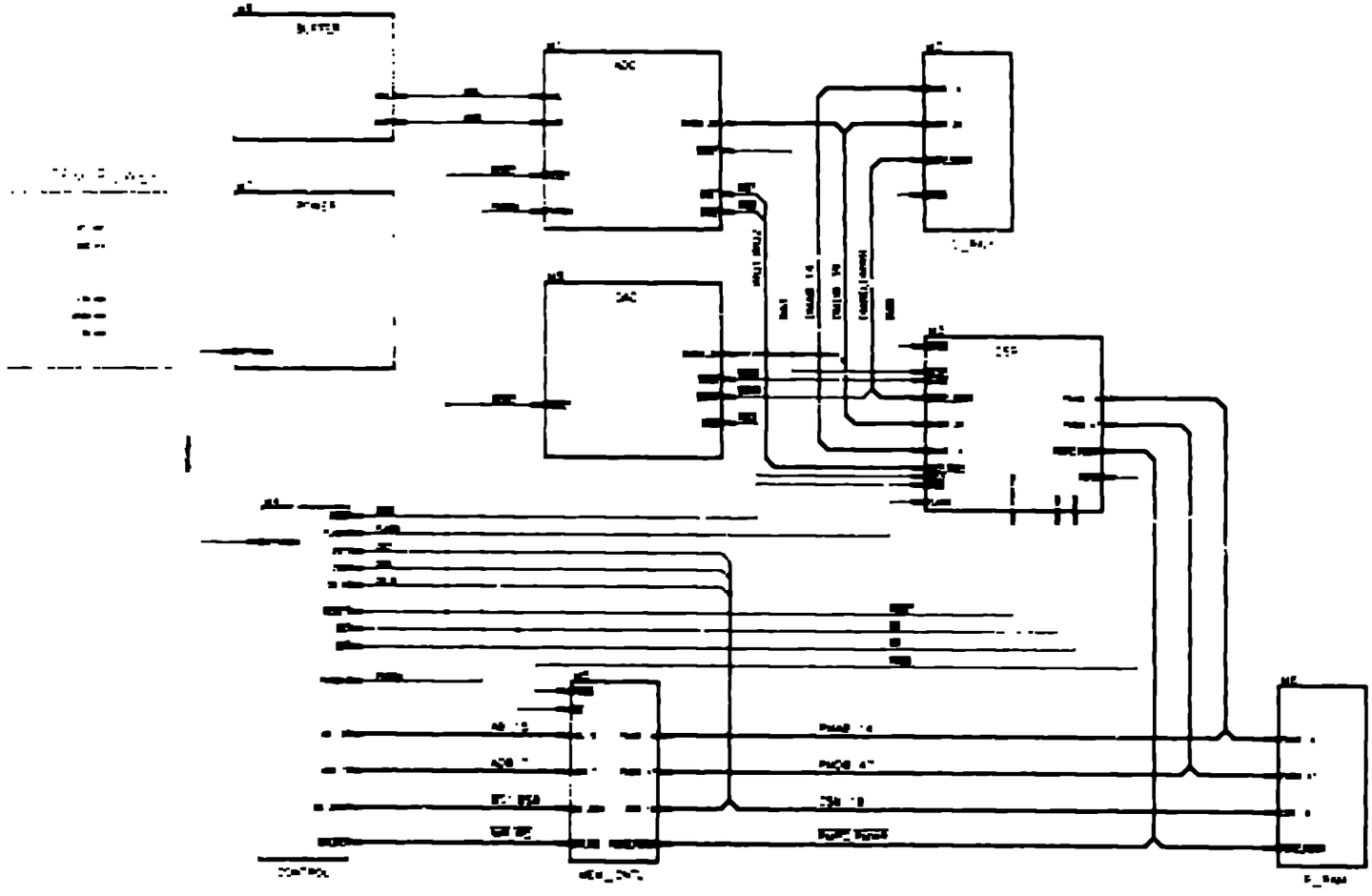

Figure 1. Block diagram of DSP/Controller board.

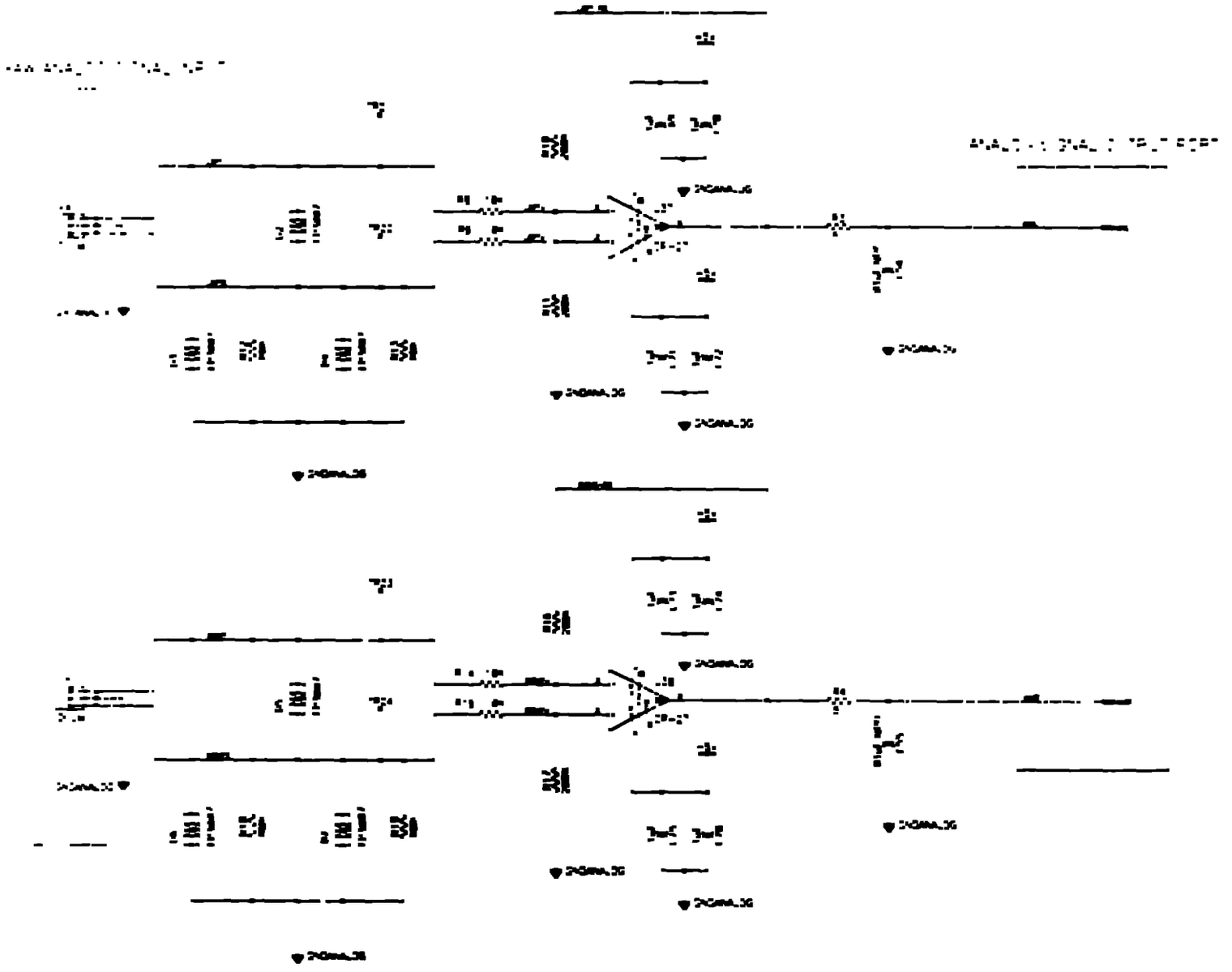

Figure 2. Front end amplifier for DSP/Controller board.

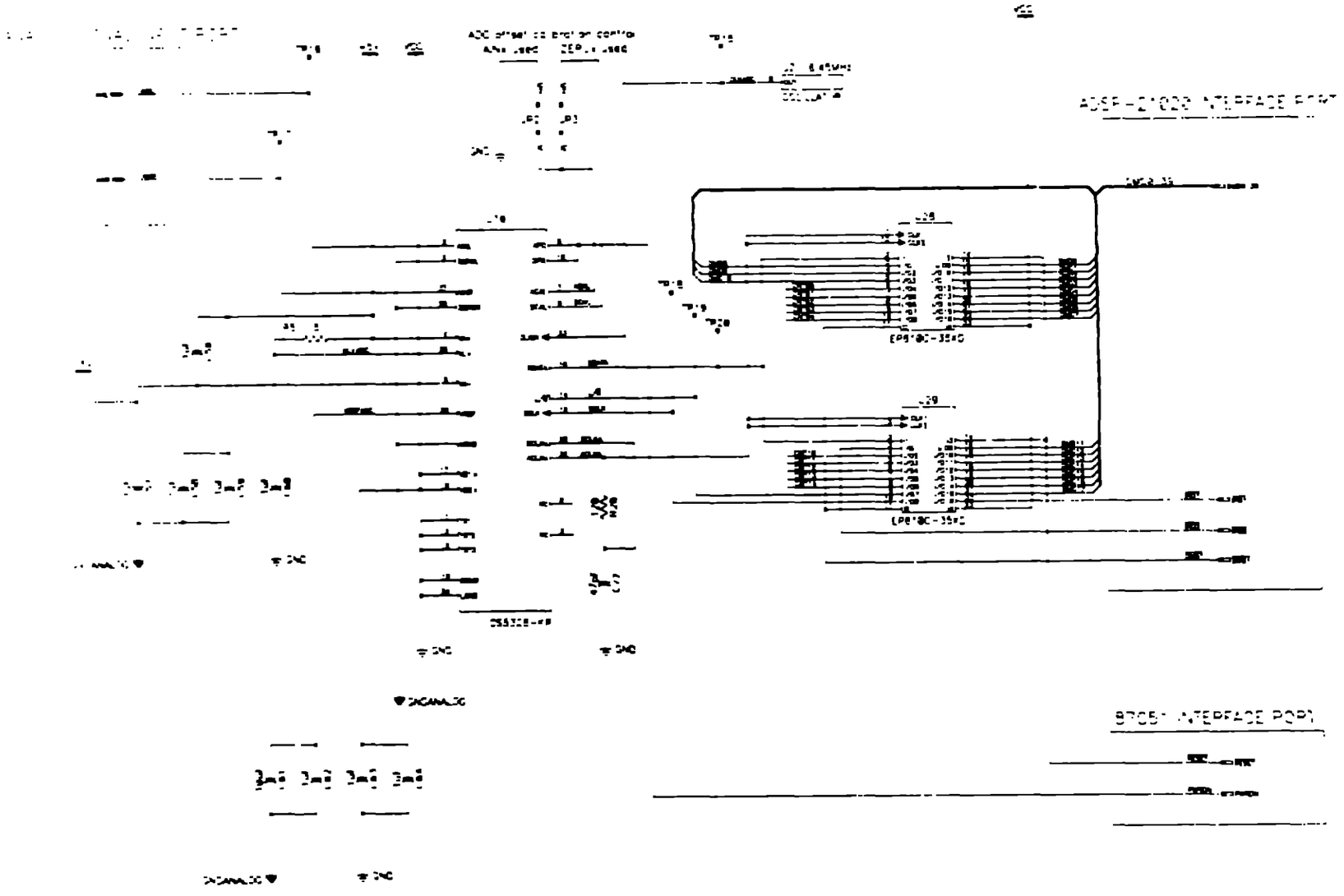

Figure 3. Analog to digital converter.

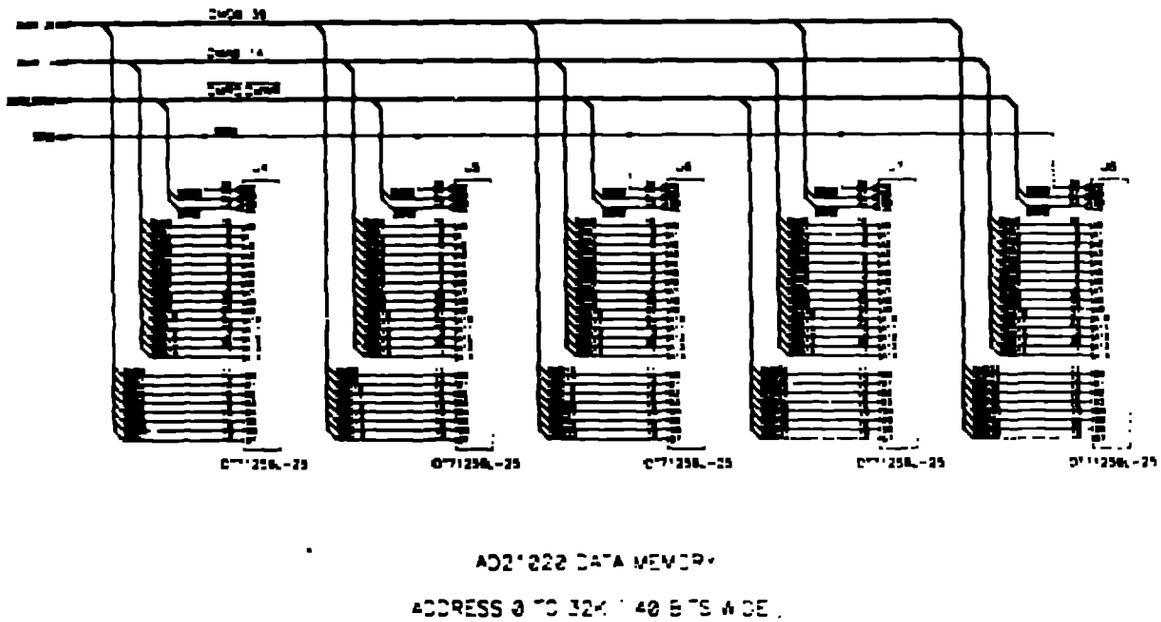

Figure 4. ADSP21020 data memory.

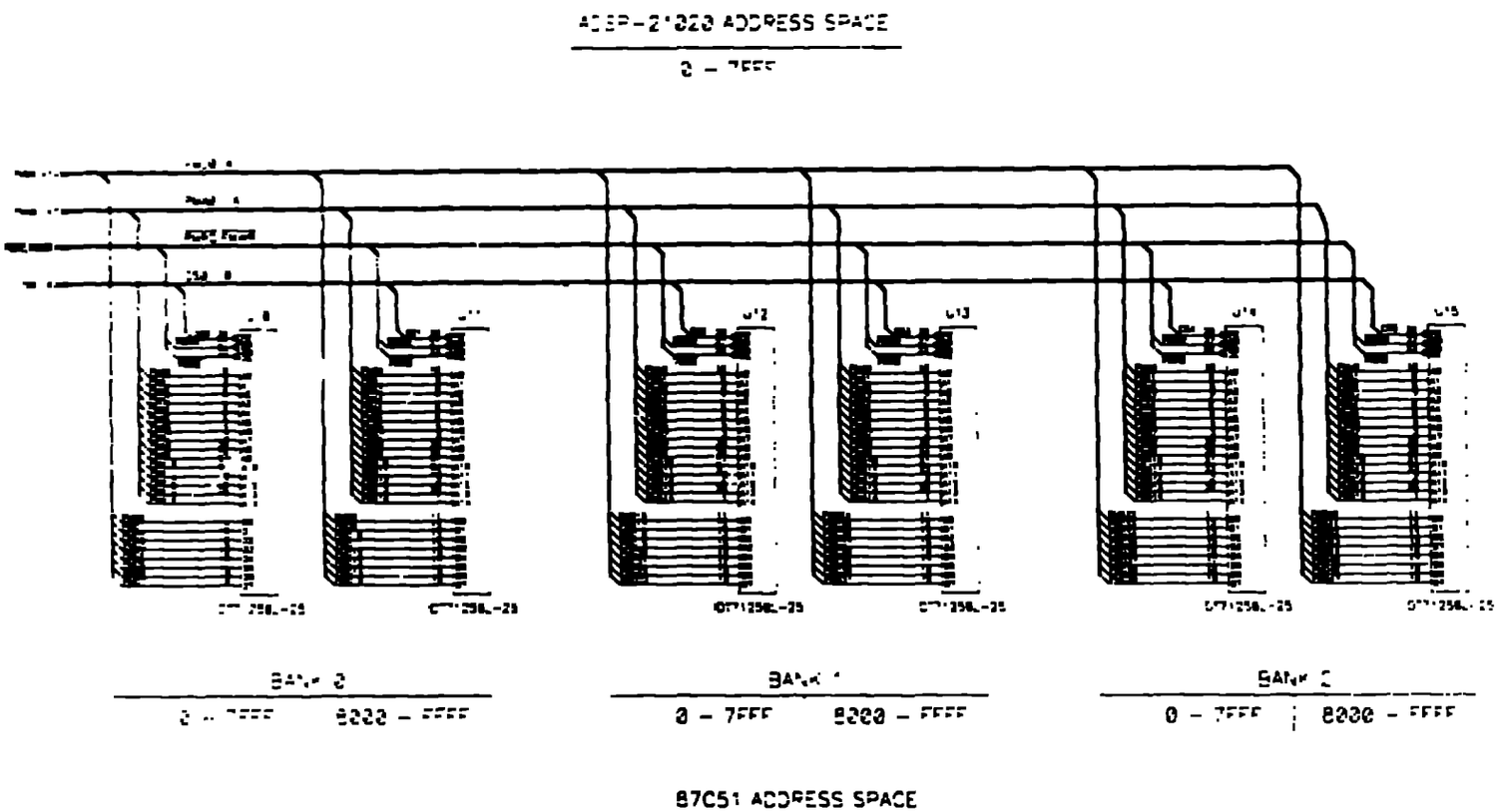

Figure 5. ADSP21020 program memory and 87C51 external data memory.

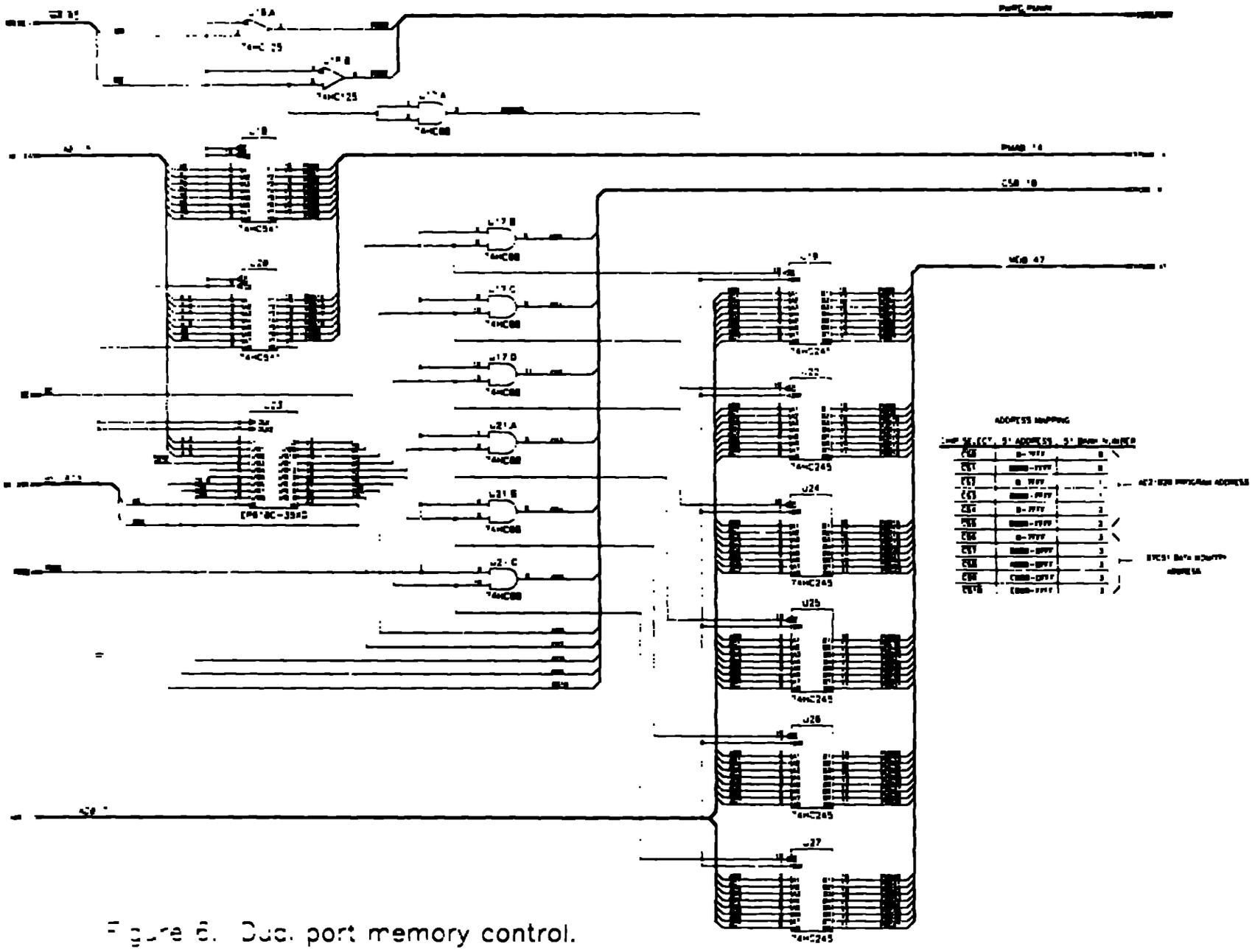

Figure 6. Dual port memory control.

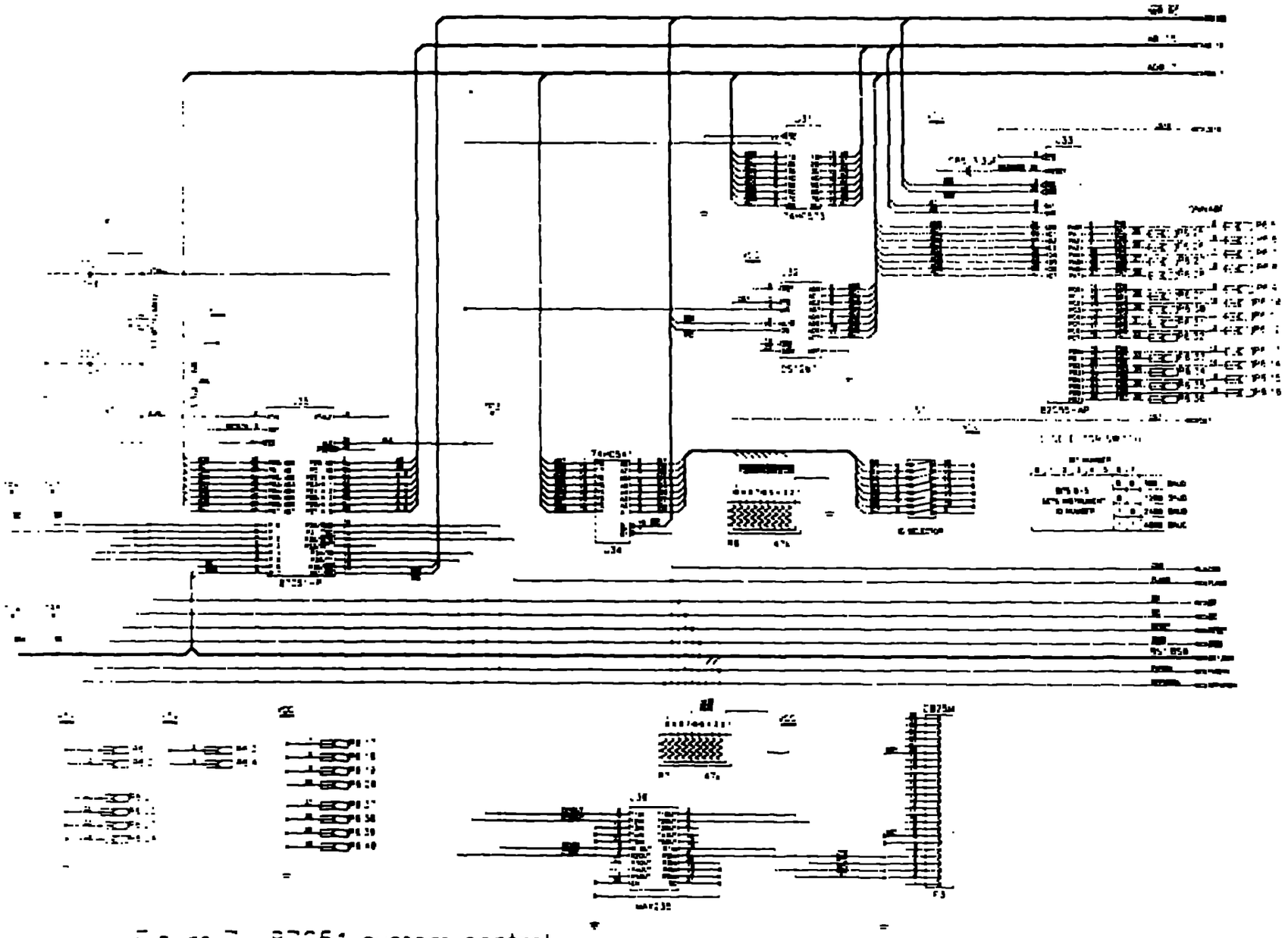

Figure 7. 8751 system control.

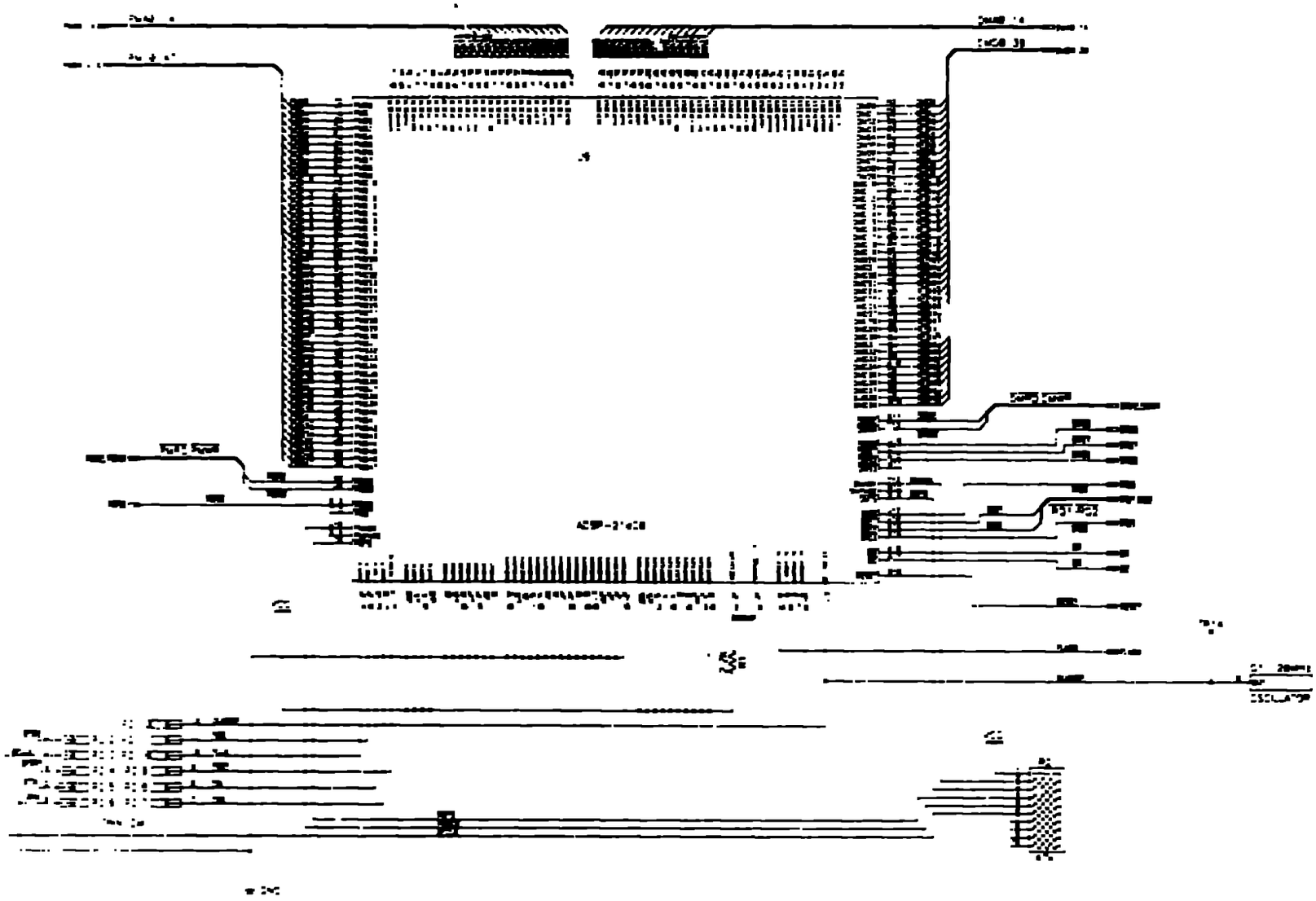

Figure 8. ADSP21020 portion of DSP/Controller board.

mode the power consumption is reduced significantly. Table II lists the system power consumption for both the DSP/controller board and the RF unit in the active and idle states. With a duty cycle of 25% total system power is approximately 5 watts; 2.6 watts for the DSP/controller board and 2.4 watts for the RF unit.

TABLE II
SYSTEM POWER CONSUMPTION

Active (Watts)	Idle Power (Watts)
18	.75

IV. Summary

Using the Analog Devices ADSP-21020 DSP has provided the basis for a low power remote CW Doppler radar. Design of the DSP/controller board was simplified because of the architecture of the ADSP-21020. Data and program memory, A/D and D/A converters, and the addition of an 8-bit microcontroller were accomplished without the need to use complicated or exotic components. Dual-porting the DSP program memory allows program code to be developed and tested without having to remove parts from the remote radar unit. A/D and D/A converters and a large program and data memory space allow for uses other than radar operation.

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