Title: Ultra-high speed hybrid CMOS imager for multi-frame proton radiography

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Ultra-Fast Hybrid-CMOS Imaging System for Multi-Frame Proton Radiography

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The performance of 4-Mframe/s burst-mode imager with 3-frame in-pixel storage will be evaluated. The 720×726px ultra-fast hybrid FPA and camera were fabricated by Rockwell Scientific (now Teledyne Imaging Sensors). Multiple cameras have been in operation for several years, in a variety of static and dynamic experiments at the 800MeV proton radiography (pRAD) facility at the LANL LANSCE accelerator. The cameras can operate with per-pulse adjustable inter-frame time of 250ns to 2s, with an exposure/integration-time as short as 180ns. With a 70 ms readout time, it can be externally synchronized to 0.1-to-5Hz, 50-ns wide proton beam pulses, and record 1000-frame radiographic movies of 5-to-30 minute duration (still with 180ns or longer shutter time). The effectiveness and dependence of the global electronic shutter on the pixilated Si-sensor bias voltage will be discussed, and compared to a “commercial” fast CMOS camera. The spatial resolution dependence of the imaging system on various monolithic and “structured” scintillators and phosphor screens will be described.

We will also present features of a new-generation 10-frame 1024x1024 pixel, 50-ns shutter, 12-bit dynamic range imager, which is now in a final design stage.

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Keywords: high-speed multi-frame radiography, fast hybrid CMOS cameras, scintillators for imaging
Ultra-High Speed Hybrid CMOS Imagers for Multi-Frame Proton Radiography

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Proton Transmission Radiography

- **Probing particles**: high-energy protons $E = 800\text{MeV}$ to $70\text{GeV}$
  - highly penetrating - inter. length $\lambda_p = 194 \text{ g/cm}^2$ (17cm) in Pb
  - image smaller dynamic range than in x-ray radiography
- **Proton flux attenuation**: nuclear collisions and multiple Coulomb scattering
- **Magnetic lens** forms Image of the Object on scintillator $1:1$, or
- **Magnifier** magnets provide - $\times3$ and $\times7$ magnification
- **Multiple beam pulses** serve as a strobe pulses: 2-to-1000 bursts; each ~ typ. 50ns wide; can be adjusted 0.3ns -100ns $\rightarrow$ motion burl; multiple views of a fast-evolving object (a movie); or tomography of static object
- Needed **camera system** with large multi-frame capability (burst mode), flexible precise triggering (independently vary inter-frame time and shutter width), high-resolution ~1-2Mpx, high QE, large pixels, radiation resistance

Seven Gated-CCD System (before 2005)

- **Full Well Saturation**
  - @ $3 \times 10^{10}$ p / burst
  - or $10^7$ p / mm²

**Resolution**

- ~1.5 lp/mm

**Thin Scintillator**

- 2mm thick (12cm x 12cm)

**Tiled LSO Scintillator**

- 25k ph/MeV, 22.5k/p

**800 MeV Proton Beam**

- Turning Mirror (8μm thick pellicle)

- Nikon 105mm/ F#2.0

- 10kV Gated Planar Diode

- Cooled CCD (1Mpx or 2.5Mpx)

- 0.6 pe/p

- **DQE** = \(1/(1+1/n)\)
  - = \(1/(1+1/0.6)\)
  - = 0.4

**Path to Hybrid-CMOS camera**

- until 2004 pRAD used 11 OE-gated single-frame CCD cameras, and two low-resolution 9-frame Framing cameras (all suffered from: low DQE, limited number of frames, min. shutter width ~320ns, FPN noise due to FOB)
- in 2003-2004 designed and fabricated a hybrid 720x720, high-QE, three-frame imager
- Hybrid CMOS ⇒ high QE and optical fill factor, well established fast CMOS technology, radiation resistant
Imager as Two-Component Hybrid Focal Plane Array (FPA)

- Independent optimization of detector and readout IC
- ~100% optical fill factor
- Arbitrarily large well depth

(1) Photo-Sensor Pixel Array (photon-charge conversion)

(2) CMOS Readout IC (ROIC): charge-to-voltage conversion, signal storage & processing, logic and A/D conversion; SoC: photons-to-bits

Cross-Sectional View

Each pixel in PD Sensor Array bump bonded (dia. < 10μm) to corresponding pixel in ROIC

ROIC Pixel layout, Metal Layer-4

Charge storage capacitors (Metal-Insulator-Metal)
- size dictated by S/N and rate of charge leakage.
- 26μm pixel footprint allows 3-frame storage, but 22mm CMOS reticle limits the ROIC size and array resolution to 720 × 720 px

to bump bonding pad

26 μm
3-Frame Storage and Correlated Double Sampling (CDS) at Pixel Level

SF front-end - saturation determined by node capacitance: $C_0$
Voltage droop on C1 – C3 by FET leakage (sub-threshold) and quality of oxide

Wafer to Hybrid FPA Chip

200mm - dia. wafer with 48 CMOS ROIC dies. Foundry delivered 12 wafers

21.4mm×22mm FPA is 2-side buttable - makes possible 1440×1440 px imager in a tiled assembly
**System-on-Chip (SoC) Architecture Simplifies Camera Integration**

- FPA chip needs only external power, master clock and trigger signals.
- The imager requires dual (3.3V and 2.5V) power supplies, “high voltage” detector bias (15V)
- The chip sends out 12 bit digital video data.
- Readout timing and biasing are generated on-chip and can be programmed through a serial interface.

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**Rockwell/ Teledyne pRAD Cameras**

CMOS ROIC fabrication worked on 1st iteration

Jan 2005, prototype –in Alu housing

Sizable volume taken up by TEC cooler and fan

Camera in stainless-steel Dewar
Silicon PD Array Has Advantages Over Monolithic CMOS or CCD’s

- 100% Fill factor (back-side illuminated)
- >95% Peak QE (AR coating)
- Good spatial and fast temporal response (fully depleted)
- Low inter-frame cross-talk /good extinction ratio (storage node isolation)
- Broad band spectrum response (deep depletion ~100μm)

Hybrid Burst Mode Imager

- Number of frames: 3
- Min. Shutter time: 150 ns (40ns)
- Inter-frame time: 250 ns
- Array Size: 720x720
- Dynamic Range: 11-bit (12-bit ADC)
- Read Noise: 98 e⁻
- Well depth: >200ke⁻
- QE: 84% (at 415nm)
- Pixel size: 26μm
- Chip size: 21.4mmx21.9mm
- CMOS technology: 250 nm
Effectiveness of Shutter Gate

Data taken with a 70ps wide, 404nm blue laser pulse. Shutter gate 400ns wide, at two bias voltage settings.

Leading Edge Dependence of Shutter Gate

The effective rising edge is longer than the expected carrier collection time (16ns, 11.8 ns and 10.1 ns for 11V, 15, and 17.5 V bias). Carrier plasma and trapping effects in detector.

However, the detector bias has remarkably little effect on the spatial resolution, as long as $V_{\text{full deletion}} \leq V_{\text{bias}}$.
Dependence of System Resolution on Scintillator Type and Thickness

Edge-Resolution vs. Scintillator Thickness referred to object (×2.7 Magnifier)

Decay times: CsI(Tl) 1us, LSO - 42ns, and EJ-208 plastic scintillator - 2.3ns

pRAD-1 Hybrid CMOS Cameras - limitations

- **spatial resolution** (at IL1) at 720×720 px and 12×12cm FOV camera is limiting the spatial resolution (in the image/scintillator plane: \( \sigma = 180\mu m \))
- **exposure time** and inter-frame time are both scintillator- and camera-limited (beam intensity) (2.3ns plastic scintillators help, but poor spatial resolution)
- **number of views** high-resolution frames pRAD is camera limited to 23 (19-frames at IL1, 4-frames at IL2)

\( \Rightarrow \) New hybrid CMOS imager is to address those issues (e.g., no. frames at IL1 for 6 cam’s \( \times 10 = 60 \))
Hybrid CMOS Imager: 1st vs. 2nd generation

<table>
<thead>
<tr>
<th>Design Parameter</th>
<th>pRAD-1 Imager</th>
<th>pRAD-2 2nd Gen Imager</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum integration time (Global shutter)</td>
<td>150 ns</td>
<td>50 ns</td>
</tr>
<tr>
<td>Nominal min. inter-frame time</td>
<td>350 ns</td>
<td>150 ns</td>
</tr>
<tr>
<td>Effective Dynamic Range</td>
<td>11.4 bits</td>
<td>12 bits</td>
</tr>
<tr>
<td>Read noise</td>
<td>100 e-</td>
<td>~ 37 e-</td>
</tr>
<tr>
<td>Imaging array size</td>
<td>720×720 px</td>
<td>1024×1024 px</td>
</tr>
<tr>
<td>Number of samples/ frames</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td>Pixel pitch</td>
<td>26 μm</td>
<td>40 μm</td>
</tr>
<tr>
<td>Sensor QE @ 415 nm</td>
<td>84%</td>
<td>&gt;90%</td>
</tr>
<tr>
<td>Chip dimensions</td>
<td>21×22 mm²</td>
<td>~42×43 mm²</td>
</tr>
<tr>
<td>Optical Fill-Factor</td>
<td>~100 %</td>
<td>~100 %</td>
</tr>
<tr>
<td>Saturation level/ Well depth</td>
<td>&gt;200 ke-</td>
<td>~ 150 ke-</td>
</tr>
</tbody>
</table>

10-frame storage: Larger Pixels & Advanced CMOS

Original 26μm pixel. New large 40μm pixel + more advanced 180nm CMOS process (larger capacitance /μm²) allow to pack 10 MIM storage caps per pixel. ⇒ Large IC chip = 42×43 mm², will need reticle stitching. Impacts cost and yield.
pRAD-2 Layout – showing all layers
High “metal density” circuit

Chip of comparable size was fabricated by TIS in 0.25μm CMOS.
Only 7 dies per wafer, and the yield was less 15%.

Summary

- Burst mode 4 MHz high-resolution, high QE, 3-frame, 720×720 px, hybrid CMOS imager successfully fabricated on 1st iteration.
- This system-on-chip (SoC) approach results in a compact, reliable and low power camera
- Six cameras built and operated for several years in radiation environment
- Thick (~100 μm) detector provides high QE, up to 900nm, but affects time definition of the shutter
- LSO scintillator optimal resolution and radiation resistance, plastic scintillator faster, but worse spatial resolution (ZnO screens?)
- New 50ns, 10-frame, 1Mpx imager in the advanced design stage
- Future radiography and FEL facilities need high-resolution sub-ns imagers

Proton Radiography Experiment: SW induced Ejecta and Instabilities (into vacuum, Xe- and He-gas)

Two Proton Radiography Experiments: (1) tomographic examination of reactor fuel rod; (2) jet penetration of HE

Fast tomographic acquisition with a remotely controlled rotation stage, 180 frames, one degree rotation step, every 2 sec; CsI(Tl) scintillator.

9km/s copper jet, generated by shaped charge, impacts a cylinder of high-explosives triggering a detonation.