Title: ABBA, Small signal, Low noise, High gain, Silicon Detector Amplifier

Author(s): Jacqueline Mirabal

Intended for: Electronic/World-wide Web
The ABBA Amplifier has unique characteristics because it is being used for a silicon detector that does not have the same gain characteristics as a wire chamber detector. Therefore the amplifier had to have a high gain, and very low signal noise in order to correctly amplify the signals from the detector. The amplifier PCB was used for 16 channels of detection on the detector. The outputs of the 16 channels were needed to drive a 50 ohm ADC system.

The first two stages form an integrator with a 1pF feedback capacitor. The third stage is used as a buffer op-amp with a gain of 20x. Two low pass filter networks were also added to the schematic before and after the third stage to control the bandwidth of the circuit. To ensure the circuit micro strip lines were at 50 ohms the PCB traces were .024” and the insulating layer between the GND layer was 1.55mm. All voltage inputs to all stages used a .1uF ceramic capacitor in parallel to a 10uF tantalum capacitor for added stability and filtering. The 50 ohm output of the circuit is used to input the signals to an electronic digitizer.
The first stage of the circuit used a BF862 N-channel junction field-effect transistor in a SOT23 package. This particular FET has a high transition frequency of 715 MHz, an input capacitance of 10pF, and a noise input voltage of .8 nV/RootHz which were desirable for this circuit application.

![FIG 2 1st Stage of ABBA Circuit](image1)

The second stage of the circuit used an AD8011 Analog Devices 300MHz Current Feedback Amplifier. This device was ideal for its wide bandwidth, low distortion, low power, and high speed specifications. The 8-lead SOIC package was used to maximize circuit stability in the PCB layout application.

![FIG 3 2nd Stage of ABBA Circuit](image2)
The third stage of the circuit used an AD8099 Analog Devices Ultra low Distortion, High Speed .95 nV/rootHz voltage Noise Op Amp. This op amp has an extremely high slew rate that allowed for flexibility in the dynamic range with minimal affect on bandwidth or distortion. The 8-lead SOIC package was also used for this op-amp.

FIG 4 3rd Stage of ABBA Circuit

The ABBA Pre-Amp board requires input voltages of +12V and -5V. Fig 5 shows the power distribution circuits for the Pre-Amp board. Two National Semiconductor 3-terminal LM117 adjustable regulators were chosen because of their capability to supply the necessary output range of 2.5V and 5V. These voltage regulators require only two external resistors to set the output voltage. 499 ohm resistors were used for the 2.5V, and 237 and 715 ohm resistors were used for the +5V.

Figure 5 Power Distribution
To verify and optimize the design for the ABBA Pre-Amp, the circuit was first simulated using Top Spice; a mixed-mode, mixed-signal circuit simulation software for analog devices, digital functions, and high-level behavioral blocks. The parameters and data from the simulations are as follows:

The above plot is the Output noise of the first stage vs. frequency. The Top Spice simulation is represented by the black graphical curve. The live measured test data points are represented by the red data points on the plot. Overlaying the two results showed that they are in general good agreement.

As with the output noise vs. frequency plot the above bandwidth plot also showed good consistency between the Top Spice simulation data and the live measured data. The data has a more limited bandwidth due to an extra low pass filter stage.
The above plot shows the linear dependency of the first stage output noise vs. input capacitance.

The specifics of the circuit design were decided from this testing data. This helped determine the values of the components that had the most impact on the functionality parameters of the circuit. Specifically the filter network component values were changed in the simulations to understand how to improve the bandwidth of the circuit. There was also a 1 pF decoupling capacitor that was needed on the second stage op-amp for consistent stability of the circuit.

Changing circuit component values added understanding to the limitations of the circuit. To test the affects of the feedback resistor, the simulation in Top Spice was calculated with both a 100M ohm and 1000M ohm resistors. The results showed that the output noise is lower at low frequencies with the 1000M ohm resistor. Simulations also showed that decreasing the drain resistor value decreased the output noise at the cost of increased power dissipation in the FET. Raising the offset voltage of 2.5V@ R2 also decreased the output noise. However, this would reduce the dynamic range capabilities of the circuit.

The live test set-up included a HP 7000 Spectrum analyzer, 8440B HP Signal Generator, Tektronix PS280 DC Power Supply, a metal noise enclosure box, and a 1pF input capacitor. Initial testing proved the significance of the component tolerances on the feedback loop on the second stage amplifier. The feedback capacitor that was placed on the manufactured boards did not have the correct tolerance, and affected the gain of the circuit. The consistency of the gain characteristics of the circuit requires the feedback capacitor to have a tolerance variation of 10% or less.
The PCB layers were as follows: Top-Signal layer, 2nd-GND layer, 3rd & 4th power distribution. The 3rd and 4th layers used power planes to uniformly distribute the power throughout the board. The signal traces between connections were traced as short as possible for our low noise, high speed application. The input and output connector design consisted of a 4 point connection to GND, and shielded connectors were also used to increase stability of the circuit.

![Figure 6 PCB Layout](image)

While testing the PCB for transients, some interesting behaviors of the circuit under certain conditions were discovered. If the PCB was lying flat on the workbench and not in the enclosure then the pick up noise on the signal would significantly increase and as a result the circuit would oscillate. Ensuring the GND connection between the testing equipment and the PCB resulted in the most reliable signal integrity. Testing the PCB inside and outside of the metal enclosure disclosed that the signal integrity of the circuit did not significantly change, it was concluded that a noise enclosure would not benefit these data acquisition efforts.

In summary the calculated cost per channel is $200. This cost includes PCB fabrication, components, and assembly. This cost could be reduced by 30% if the quantity of boards is increased above 20, and the requested delivery date is more than 10 working days. The final output noise of the first stage is 22nV/root Hz at 22pF input capacitance, which is equivalent to an input noise of 1nV/root Hz at 10MHz. The live and simulation data are consistent with one another and verify the concept and final design of the amplifier for Silicon Detector data acquisition.