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Solar Agile Delivery of Electrical Power Technology (Solar ADEPT)

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Abstract

This talk is for the ARPA-E funded program that Los Alamos is part of a team with Carnegie Mellon University, Magnetics div. of Spang, and the University of Pittsburgh. Most of the material presented in this talk has been presented before and is associated with accelerators and has a “DUSA” “ATDO” designator. Slight variations in circuit topology as presented here are somewhat novel and although not classified should be considered Los Alamos proprietary. The viewgraphs from “both” talks will be presented to team members and the ARPA-E sponsor.

Topology Overview

- The power circuit topology presented here is new and unpublished so should be treated as Los Alamos National Laboratory **proprietary**
- The AM Resonant link (AMRES-link) Inverter is based on a series resonant parallel loaded converter configuration.
- Soft switching and dynamic regulation is achieved using Combined Phase and Frequency Modulation (CPFM)

Input H-Bridges

Medium Voltage (13.8kV) Output Side (Single Phase)

Key Features and Potential Benefits

Potential Benefits

- All MOSFET devices switch softly under all operating conditions
- Output devices switch at 50/60Hz
- Low dv/dt -> EMI
- Simple to connect many modules in parallel
- Could use active filter for harmonic cancelation
- Small output filter components (6f ripple for a 3 phase system)
- No complicated bidirectional switches
- Conduction losses should be similar to that of stacked H-Bridge
- Good light load efficiency because modules can be selectively disabled

Possible Disadvantages

- Variable switching frequency on resonant tank (could be up to 40%)
- Resonant tank components may be lossy &/or expensive if the transformer parasitics cannot be used
- Unidirectional power flow
- Only possible to supply real power

PLECS Simulation Modeling Continues

- Sung Il Kwon and Alex Scheinker
- Updating model for “as-built”
- Updating model for measured values

Simple C-core Design for High Voltages

7.7 kVAC, 50 kHz, 100 kW Nanocrystalline Transformer

TRANSFORMER ASSEMBLY
EXPLODED ISOMETRIC VIEW
PCB'S NOT SHOWN

ASSEMBLY ISOMETRIC VIEW
PCB'S SHOWN

- Multi-filar Primary
- Type 2 Litz Primary
- Solid Wire Secondary
- Multi-basket Secondary

SOLAR ADEPT TRANSFORMER
(12" WIDTH X 12" DEPTH X 14" HEIGHT)
EST. WEIGHT: 30LBS - AS SHOWN WITH PCB'S

PRELIMINARY

JUNE 19, 2012

7.7 kVAC, 50 kHz, 100 kW Nanocrystalline Transformer

SOLAR ADEPT TRANSFORMER
(12" WIDTH X 12" DEPTH X 14" HEIGHT)
EST. WEIGHT: 30LBS - AS SHOWN WITH PCB'S
PRELIMINARY

JUNE 19, 2012

- SiC Mosfets
- Gate Drivers External
- Forced Air Cooled

Benchmark FT-3 Cores Ordered and Received

- Will Be Used to Evaluate Transformer Design
 - Leakage Inductance, Stray Elements
 - Back Annotate Circuit Model
 - Test Electronics
 - Benchmark Performance
- Flux concentration on ID
 - Will Return (Have RMA)

Prototype Bobbins Printed for Testing / Evaluation

- Style Used for 3 Phase Design
- Evaluate Resonant Frequency
- Evaluate Leakage Inductance
- Evaluate Winding Technique
- Used to Compare with Multi-Basket Single Phase Design
 - Multi-Basket Bobbins in Fab
 - Heavier than Model
 - not thin wall
 - “through” machined
 - 8 lbs additional

Gate Driver and Test Fixture for CREE SiC Transistor Evaluations

- Evaluating Gate Driver and CREE SiC Device
 - T_r , T_f
 - switching delay, symmetry
 - thermal performance
- Different Driver Design SemiSouth SiC MOSFET
 - depletion mode JFET
 - parts just received
 - board in fab

Preliminary Test Fixture For SiC Device Characterization

V gate

CREE Gate "On" Drive and Delay (slow)

CREE Gate "Off" Drive and Delay

I drain

We Have The Preferred SiC Device For Our Application

Silicon Carbide SJDP120R045

Normally-On Trench Silicon Carbide Power JFET

Product Summary		
BV_{DS}	1200	V
$R_{DS(on)max}$	0.045	Ω

Features:

- Positive Temperature Coefficient for Ease of Paralleling
- Extremely Fast Switching with No "Tail" Current at 150 °C
- $R_{DS(on)}$ typical of 0.035 Ω
- Voltage Controlled
- Low Gate Charge
- Low Intrinsic Capacitance

Applications:

- Solar Inverter
- SMPS
- Power Factor Correction
- Induction Heating
- UPS
- Motor Drive

MAXIMUM RATINGS

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current	$I_{D, TC=25}$	$T_C = 25\text{ }^\circ\text{C}$	48	A
	$I_{D, TC=100}$	$T_C = 100\text{ }^\circ\text{C}$	30	
Pulsed Drain Current ⁽¹⁾	I_{DM}	$T_J = 25\text{ }^\circ\text{C}$	140	A
Short Circuit Withstand Time	t_{SC}	$V_{DS} < 800\text{ V}, T_C < 125\text{ }^\circ\text{C}$	50	μs
Power Dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	208	W
Gate-Source Voltage	V_{GS}	AC ⁽²⁾	-15 to +15	V
Operating and Storage Temperature	T_J, T_{stg}		-55 to +150	$^\circ\text{C}$
Lead Temperature for Soldering	T_{sld}	1/8" from case < 10 s	260	$^\circ\text{C}$

⁽¹⁾ Pulse width limited by maximum junction temperature

⁽²⁾ $R_{g(ext)} = 1\text{ }\Omega, I_D \leq 200\text{ mA}$, see Figure 6 for static conditions

THERMAL CHARACTERISTICS

Parameter	Symbol	Value		Unit
		Typ	Max	
Thermal Resistance, junction-to-case	$R_{th,jc}$	-	0.6	$^\circ\text{C} / \text{W}$
Thermal Resistance, junction-to-ambient	$R_{th,ja}$	-	50

Silicon Carbide SJDP120R045

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	

Off Characteristics

Drain-Source Blocking Voltage	BV_{DS}	$V_{GS} = -15\text{ V}, I_D = 1200\text{ }\mu\text{A}$	1200	-	-	V
Total Drain Leakage Current	I_{DSS}	$V_{DS} = 1200\text{ V}, V_{GS} = -15\text{ V}, T_J = 25\text{ }^\circ\text{C}$	-	20	-	μA
		$V_{DS} = 1200\text{ V}, V_{GS} = -15\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	200	-	
Total Gate Reverse Leakage	I_{GSS}	$V_{GS} = -15\text{ V}, V_{DS} = 0\text{ V}$	-	-0.2	-0.6	mA
		$V_{GS} = -15\text{ V}, V_{DS} = 1200\text{ V}$	-	-0.2	-	

On Characteristics

Drain-Source On-resistance	$R_{DS(on)}$	$I_D = 30\text{ A}, V_{GS} = 2\text{ V}, T_J = 25\text{ }^\circ\text{C}$	-	0.035	0.045	Ω
		$I_D = 30\text{ A}, V_{GS} = 2\text{ V}, T_J = 100\text{ }^\circ\text{C}$	-	0.06	-	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = 1\text{ V}, I_D = 70\text{ mA}$	-	-5	-	V
Gate Forward Current	I_{GFWD}	$V_{GS} = 2\text{ V}$	-	41	-	μA
Gate Resistance	R_G	$f = 1\text{ MHz}, \text{ drain-source shorted}$	-	4	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{DD} = 100\text{ V}, V_{GS} = -15\text{ V}$ $f = 100\text{ kHz}$	-	510	-	pF
Output Capacitance	C_{oss}		-	160	-	
Reverse Transfer Capacitance	C_{rss}		-	160	-	
Effective Output Capacitance, energy related	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 600\text{ V}, V_{GS} = -15\text{ V}$	-	100	-	

Switching Characteristics

Turn-on Delay	t_{on}	$V_{DS} = 600\text{ V}, I_D = 25\text{ A},$ Inductive Load, $T_J = 25\text{ }^\circ\text{C}$ Gate Driver = +15 V, -15 V, $R_{g(ext)} = 2.5\text{ }\Omega$	-	12	-	ns
Rise Time	t_r		-	24	-	
Turn-off Delay	t_{off}		-	20	-	
Fall Time	t_f		-	22	-	
Turn-on Energy	E_{on}		-	180	-	
Turn-off Energy	E_{off}	See Figure 12	-	200	-	μJ
Total Switching Energy	E_{ts}		-	380	-	
Turn-on Delay	t_{on}	$V_{DS} = 600\text{ V}, I_D = 25\text{ A},$ Inductive Load, $T_J = 150\text{ }^\circ\text{C}$ Gate Driver = +15 V, -15 V, $R_{g(ext)} = 2.5\text{ }\Omega$	-	12	-	ns
Rise Time	t_r		-	26	-	
Turn-off Delay	t_{off}		-	20	-	
Fall Time	t_f		-	24	-	
Turn-on Energy	E_{on}		-	185	-	
Turn-off Energy	E_{off}	See Figure 12	-	215	-	μJ
Total Switching Energy	E_{ts}		-	400	-	
Total Gate Charge	Q_g	$V_{DS} = 600\text{ V}, I_D = 15\text{ A},$ $V_{GS} = +2.5\text{ V}$	-	65	-	nC
Gate-Source Charge	Q_{gs}		-	4	-	
Gate-Drain Charge	Q_{gd}		-	54	-	

Have Tested CREE SiC Device

CMF20120D-Silicon Carbide Power MOSFET
Z-FET™ MOSFET
N-Channel Enhancement Mode

Features

- Industry Leading $R_{DS(on)}$
- High Speed Switching
- Low Capacitances
- Easy to Parallel
- Simple to Drive
- Pb-Free Plating, RoHS Compliant, Halogen Free

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Avalanche Ruggedness
- Increased System Switching Frequency

Applications

- Solar Inverters
- High Voltage DC/DC Converters
- Motor Drives

Package

TO-247-3

Part Number	Package
CMF20120D	TO-247-3

V_{DS}	= 1200 V
$R_{DS(on)}$	= 80 mΩ
$I_{D(MAX)}$ @ $T_C=25^{\circ}C$	= 33 A

Maximum Ratings

Symbol	Parameter	Value	Unit	Test Conditions	Note
I_D	Continuous Drain Current	33	A	$V_{GS}@20V, T_C = 25^{\circ}C$	
		17		$V_{GS}@20V, T_C = 100^{\circ}C$	
I_{Dpulse}	Pulsed Drain Current	78	A	Pulse width t_p limited by T_{jmax} $T_C = 25^{\circ}C$	
E_{AS}	Single Pulse Avalanche Energy	2.2	J	$I_D = 20A, V_{DD} = 50 V,$ $L = 9.5 mH$	
E_{AR}	Repetitive Avalanche Energy	1.5	J	t_{AR} limited by T_{jmax}	
I_{AR}	Repetitive Avalanche Current	20	A	$I_D = 20A, V_{DD} = 50 V, L = 3 mH$ t_{AR} limited by T_{jmax}	
V_{GS}	Gate Source Voltage	-5/+25	V		
P_{tot}	Power Dissipation	150	W	$T_C=25^{\circ}C$	
T_j, T_{stg}	Operating Junction and Storage Temperature	-55 to +125	$^{\circ}C$		
T_L	Solder Temperature	260	$^{\circ}C$	1.6mm (0.063") from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw

I out

V gen

100 kHz & 8 Amps

DC-AC Resonant Converter with Combined Phase/Frequency Modulation

Alexander Scheinker, Sungil Kwon, Michael Bland, Bill Reass, Mark Prokop

Control Problem Overview

We consider the problem as that of robust control for optimal output performance of a nonlinear dynamic system with two unpredictable, independent, time-varying components:

- Solar panel output power, $s(t)$, available for sampling, with dynamics based on unknown function.
- Grid fluctuation due to usage, $g(t)$, also available for sampling, with dynamics based on unknown function.

$$\begin{bmatrix} \dot{x}_1 \\ \vdots \\ \dot{x}_n \end{bmatrix} = \begin{bmatrix} f_1(x_1, \dots, x_n, u, s, g, t) \\ \vdots \\ f_n(x_1, \dots, x_n, u, s, g, t) \end{bmatrix}$$

Dynamic system with states $x_i(t)$ (various voltages, currents, output power...) and control $u(t)$.

$$u = u(x_1, \dots, x_n, s(t), g(t))$$

Feedback control, $u(t)$, based on grid and solar panel readings as well as system state measurements.

$$\dot{s}(t) = f_s(t), \quad \dot{g}(t) = f_g(t)$$

Solar panel / grid outputs based on unknown, dynamic, time-varying systems (sun, clouds, usage...).

Single Phase System Overview

Initial Single Phase Controller Setup

Combined phase and frequency modulation for zero voltage / zero current switching.

Initial controller based on standard phase-locked loop techniques, combined with phase/frequency modulation.

Initial Controller Results

Initially non-zero switching.

Initial Controller Results

Zero switching quickly achieved by feedback controller.

Initial Controller Results

50kHz switching = compact transformer.

Initial Controller Results

IGBT Currents

Diode Currents

Output current/grid voltage ($P=IV>0$),
power to grid.

General Three Phase Setup

General Three Phase Setup

Three phase requires more sophisticated controller (Initial development on single phase system), choices considered:

- Model independent extremum-seeking
- Neural network
- System/Parameter ID

Preliminary 3 Phase Results

Concluding Remarks, 2nd Quarter Results

- Resonant Topology Chosen
 - Multifilar dual drive double basket topology
 - Minimizes EMI
 - Minimizes component stresses
 - core harmonics / losses
 - switch recovery
 - can tune out parasitics
 - Soft switching improves semiconductor frequency capabilities
 - Option to select windings dependant on power
- Modeling Combined Phase and Frequency Controls
 - Developing DSP algorithms
 - Developing Extremum-Seeking Controls
- Updating PLECS Model to Circuit Values from Prototypes
- Testing and Evaluating Components
 - Testing Circuit Designs
- All Critical Components Received
- Assemblies in Production