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Flight Experience of the Xilinx Virtex-4

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Background

- **The Xilinx Virtex-4 field-programmable gate array (FPGA) has been studied by several organizations for use in space applications.**
 - Launched into low-earth orbit (LEO) by Sandia National Laboratories and the National Aeronautics and Space Administration (NASA).
- **Los Alamos National Laboratory (LANL) launched an experimental payload, called the Mission Response Module (MRM), on a Department of Defense satellite in FY11.**
 - The MRM system has two units: Los Alamos Experimental Units (LEUs).
 - Each LEU includes two Xilinx Virtex-4 FPGAs: one XQR4VLX200 and one XQR4VSX55.
- **This talk will highlight results from the first year in orbit.**

The MRM System

- **The two FPGAs are scrubbed using an Actel RTAX FPGA.**
 - The scrubber algorithm has a frame-based read back and repair methodology.
 - Each FPGA's configuration memory is continuously read.
 - Scrubber only repairs single frames of data as SEUs are detected.
 - Information about the single-event upsets (SEUs) and single-event functional interrupts (SEFIs) are time stamped and returned to the ground station for further analysis
- **LANL pre-deployment testing included a validation of the scrubber using 63.3 MeV protons to ensure proper scrubbing**

- Operated by Los Alamos National Security, LLC for the U.S. Department of Energy's NNSA

Pre-Launch Predictions

- **Information from Greg Allen's "Virtex-4QV Static SEU Characterization Summary" was used to calculate the CREME96 predictions**
 - For this orbit, CREME96 predicted a combined FPGA SEU rate of 68-89 SEUs/device-day for each LEU, depending on solar conditions.
 - Each Virtex-4 should have an observable output error approximately every 15 to 25 days.
- **There was some concern before launch that MBUs could limit the effectiveness of TMR.**
 - LANL test results indicated that $3.25\% \pm 0.05\%$ of all SEUs caused by 63.3 MeV protons would be MBUs.
 - Configuration memory could have up to $6.75\% \pm 0.10\%$ MBUs.
 - In heavy ions, the MBU rates could be much higher.
- **There was also no way to predict the MBU rate before launch.**

Observed SBUs and MBUs

- **Most of the SEUs are in the SAA**

- Red dots are the MBU locations, green dots are the SBUs.
- Mid- and high-latitude areas are starting to fill in over the year.
- Southern polar cap mostly absent due to earlier operational issues, but continue to be slow to fill in.

On-Orbit SEUs and SEFIs

- During this time period the two LEUs have seen a total of 3,170 SEUs between the four FPGAs.
 - The LX FPGA has 14.5 SEUs/device-day $\pm$ 0.07 SEUs/device-day.
 - The SX FPGA has 5.2 SEUs/device-day $\pm$ 0.08 SEUs/device-day.
- There have been three SelectMAP SEFIs.
 - The worst-case predictions for SelectMAP SEFIs is every 26 years.
 - Scrubber responded correctly when SEFIs occurred and processing was restarted within a minute

Comparison of Predictions to CREME96

- For the same time period, CREME96 predicted that the number of SEUs for the two LEUs should have been four to five times higher than the actual SEU rate.
- This result is consistent with our experience with flying the Cibola Flight Experiment (CFE) and other organizations' experience with their deployed Xilinx Virtex family components, but we have examined whether our uptime in the SAA or shielding could possibly have on these results.

Corrections to the CREME96 Predictions

- We noticed during the turn-on phase of the payload occasional days where the ratio of the actual to predicted SEUs above 100%, which were caused by the payload being disproportionally scheduled for the SAA.
- We also noticed in March 2012 that there was regular per-orbit maintenance work occurring in the southern part of the orbit, causing the payload to be off during the southern portion of the SAA.
- We determined that the payload spends on average 39% of all uptime in the SAA
- From this analysis we have found the ratio of actual to predicted SEU rates is on average 52%.
- There is a significant amount of shielding to one side of the payload (up 10 inches of Aluminum), which could be cutting down on the environment from that side of the spacecraft.

Ratio of Actual to Predicted SEUs in SAA

Observable Output Errors

- **Because the actual SEU rate is much lower than predicted SEU rate, the time between observable output errors should also increase.**
 - The original estimate is from 15-25 days based on 68-89 SEUs/device-day
 - The more realistic estimate is 75-125 days based on 19 SEUs/device-day
- **There have been four output errors since October 2011.**
 - The current rate for output errors is once every 49 days with a 95% confidence interval of (48 days, 52 days) between output errors.
- **As expected, the payload is immune to over 99% of the SEUs that occur in the FPGAs.**

Observed MBUs

- **We determined that $7.22\% \pm 0.76\%$ of the on-orbit SEU events are MBUs.**
 - None of the output errors have been tied to MBUs.
- **The data from all of the FPGAs is consistent with normal incidence 63.3 MeV proton tests.**
 - Originally there was an anomalously high MBU rate on the SX components, which has been blunted in the recent months by an increase in the number of MBUs.
- **On average $85\% \pm 15\%$ of the MBUs are 2-bit upsets.**

Component	MBUs
LEU1 LX	$7.59\% \pm 1.13\%$
LEU1 SX	$7.35\% \pm 1.32\%$
LEU2 LX	$6.51\% \pm 2.06\%$
LEU2 SX	$5.19\% \pm 2.41\%$

Size of Event	Percentage of Event
2-bit	$84.83\% \pm 14.66\%$
3-bit	$7.36\% \pm 2.86\%$
4-bit	$5.31\% \pm 2.35\%$
5-bit	$0.86\% \pm 0.84\%$
6-bit	$1.54\% \pm 1.15\%$

Memory Types

- While the FPGA's memory is made of standard SRAM cells, the memory cells are laid out in three feature sizes.
- From testing, we have found that these different memory cell layouts have subtly different sensitivities to radiation.
- On orbit we have found that upsets occurred in these areas of the programming data:
 - $65\% \pm 3\%$ in configuration logic blocks (CLBs)
 - $30\% \pm 1\%$ in BRAM interconnect, and
 - $3\% \pm 1\%$ of the SEUs occurred in the input/output blocks
 - Data on the BlockRAM is not available as it is not being monitored for SEUs.
- Most of the SEUs affect routing resources.
 - $78\% \pm 5\%$ of the SEUs occur in the programmable routing used to connect the programmable logic.
 - $11\% \pm 1\%$ of the SEUs occur in the programmable routing used to interface to the hard cores, such as the digital signal processing units and the BlockRAM
- SEUs in the programmable logic, which consists of lookup tables (LUTs), comprise $6\% \pm 1\%$ of the SEUs.

Conclusions

- **We have presented on-orbit results from a deployed Virtex-4 system from October 2011 to August 2012.**
- **These early results show that the CREME96 predicted SEU rate is four to five times higher than the actual SEU rate.**
 - The SEU rate might be artificially low due to the amount of time the payload is operating in the SAA and the amount of metal to one side of the payload.
 - The MBU rate is $7.22\% \pm 0.76\%$ of all SEUs.
- **The system is immune to 99% of the SEUs that occur, due to mitigation.**